All Graphene Nano Ribbon on Diamond Substrate Energy Efficient Power Electronics Switch

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In order to meet current and emerging needs and deliver future force capabilities the US Army needs to develop and implement the most sophisticated energy efficient power electronics technologies. This white paper focuses Army's stated need for "increasing forces' freedom of action through energy security and efficient power systems to provide desired power at the manned/unmanned platforms, at the system and personal levels". Army requires "efficient and secure power systems for the forces to provide the required power when and where needed with great deal of reliability." The existing power electronics systems are based on traditional metals, like copper and aluminum and traditional semiconductors. They cannot provide the future needs of the Army. Hence there is a need to develop a new technology based on covalent bonded materials like graphene.

Insatiate demand for miniaturization of power electronics requires a substantial reduction in the dimensions of the components used in power electronics (such as metal interconnects and solder joints). At the same time, due to demand for faster and more functional power electronics that can operate at higher temperatures, there is an evolution toward higher voltages and also higher power densities. These requirements lead to high current density in these components ($>10^6 Amp/Cm^2$). Physical limits to increasing the current density – and limiting further miniaturization- in metals are electromigration and thermomigration phenomena. Electromigration in interconnect metal lines, and solder joints is the major failure phenomenon in next generation power electronics As result there is a need to develop the next generation power electronics by replacing the traditional metals, with covalent bonded materials like Graphene Nano Ribbon which do not experience electromigration and thermomigration in the traditional sense.

The technology proposed in the white paper was developed by ONR funding in the last 10 years and recently January 2020, was patented by USPTO. However, there is a need for funding to develop technology needed to manufacture it. Because it was funded by US Navy, our patent requires US based manufacturing. Depending on the funding level this device can be made available to US Army in 5 to 7 years.

Electrostatic Doping-Based All GNR Tunnel FET: An Energy-Efficient Design for Power Electronics

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***Abstract*— Electrostatic doping (ED)-based graphene nanoribbon (GNR) tunneling field-effect transistor (TFET) with trigate design is studied. The transfer and output characteristics of the GNR-TFET are explored using extended Hückel semiempirical method. An I_{ON}/I_{OFF} ratio as high as 10^{14} is obtained with the ON-state current on the order of 10^3 μA/μm. A sub-60 mv/decade subthreshold swing is also observed (35 mv/decade). Armchair GNR with widths of 11 and 9 dimmers is found to be the best geometry to obtain a high I_{ON}/I_{OFF} ratio, and channel length of greater than 6.9 nm suppresses short-channel effect. The scaling behavior of the ED-based GNR-TFET is also studied. It is observed that a smaller gate-to-gate distance facilitate large ON-state current and small OFF-state current. Moreover, it is shown that for a high-quality switching performance, the lowest required built-in gate voltage must provide enough energy differential ΔE between the source- and drain-side energy bands.**

***Index Terms*— Electrostatic doping (ED), graphene nanoribbons (GNR), nonequilibrium Green's function (NEGF), power electronics, tunneling transistor.**

I. Introduction

GRAPHENE has been intensively studied due to its exceptional mechanical, electrical, and thermal properties [1]–[5]. Since 2007, a significant amount of research effort has been made toward the application of graphene and graphene nanoribbon (GNR) in MOSFET as the conduction channel [6], [7]. However, the use of graphene/GNR in MOSFET still suffers from the drawback of high-power consumption at the OFF-state. Which is reflected in its unreducible subthreshold swing (SS) below 60 mV/decade at room temperature [8]. As the size of MOSFET scales down, and threshold voltage is lowered, the leakage current at OFF-state increases exponentially, giving rise to significant static power consumption.

In seeking of energy-efficient transistors while keeping the advantage of graphene/GNR, researchers have started to explore the possibility of graphene/GNR-based tunnel field-effect transistor (TFET), where its conduction of carrier relies on the interband tunneling, and thus, a SS of sub-60 mv/decade is possible.

In TFET, one of the most critical issues is the creation of a p-i-n (n-i-p) junction in the channel, where the p, n, and i denote the p-/n-type doped region and the intrinsic region, respectively. For silicon-based TFET, this could be readily done by chemical doping. However, unlike bulk silicon, graphene has a 2-D structure and its doping techniques are more complicated and challenging. Several groups have prepared boron and nitrogen-doped graphene via chemical vapor deposition [9], [10]. However, doped single-layer graphene was only occasionally detected and the measured mobility is less than 500 $cm^2 \cdot V^{-1} \cdot s^{-1}$, which is unacceptable for real application of graphene or GNR as the transistor channel. Due to the immature graphene doping techniques, to the best of our knowledge, no research group so far has successfully prepared the graphene or GNR-TFET p-i-n (n-i-p) channel via chemical doping.

On the other hand, graphene/GNR-TFET has been studied using theoretical models. Chin *et al.* [11] had studied the transfer characteristics of GNR-TFET using nonequilibrium Green's function (NEGF). They found that the lower drain doping concentration would enhance I_{ON}/I_{OFF} ratio, while higher source doping concentration would enhance I_{ON} but degrades the SS. Zhang *et al.* [12] proposed a GNR-TFET model with p-i-n channel, and they predicted an ON-state current density as high as 800 μA/μm, with I_{ON}/I_{OFF} ratio of more than 10^7. In their calculation, they also predicted that the lower limit of SS can be as small as 0.19 mV/decade. In these previous studies, however, very little information was discussed about the doping techniques to create the p- and n-type regions in the graphene/GNR-TFET channel. In the literature, for simplicity, doping is assumed to be realized with a certain amount of charge compensation without specifying any dopant source. Although such an approach would work theoretically, it fails to provide a feasible doping technique and, thus, creates a gap between theory and real-world application.

Here, we use a feasible doping technique: the electrostatic doping (ED), which employs an electric field to continuously tune the position of Fermi level from the mid gap to conduction band (CB) (n-type doping) or valence band (VB) (p-type doping). Without the introduction of dopant atoms, the monolayer structure and high carrier mobility feature of GNR can be preserved by ED. Thus, we believe ED is promising in GNR-TFET applications.

In 2004, ED has been used in carbon nanotube TFET [13] in which additional gates are used to create electrical fields

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for the doping, and an SS of sub-60 mV/decade is observed. Recently, Hamam *et al.* [14] used ED to GNR-TFET and studied experimentally the viability of ED-based GNR-TFET and measured the I_D–V_G response at different temperatures. However, in their studies, the chirality and defect density of the GNR are unknown, which both have huge influence on the electrical properties of the GNR. Moreover, since they used very wide GNR as the channel (∼10 nm, and thus a small bandgap of ∼70 meV), they observed very low I_{ON}/I_{OFF} ratio of 10^3 at 5 K and only 20 at 300 K.

In order to find the optimal performance of ED-based GNR-TFET, a systematic study is required. Here, we present a comprehensive study on the scaling behavior of ED-based GNR-TFET. The layout of this paper is as follows. First, we present the device configuration and simulation approach. Then, we discuss the channel length and width effect on the I_D/V_{MG} transfer characteristics. In addition, we also discussed the influence of gate-to-gate distance and the influence of the built-in voltage, which are unique aspects of ED-based GNR-TFET and are never studied in the literature. Finally, we studied the effect of supply voltage on the transfer and output characteristics. Through modifying the channel and gate geometries as well as the ED level, we highlight the guidelines for optimizing the performance of ED-based GNR-TFET devices. We show that I_{ON}/I_{OFF} ratio as high as 10^{14} is possible with the design we proposed.

II. Device Configuration and Simulation Approach

The ED-based GNR-TFET consists of five regions: a finite intrinsic channel where carriers are transported through, n-type doped source and p-type-doped drain, two semiinfinite electrodes and their extensions, metallic gates, and dielectric insulator between the gates and the GNR. A trigate design is employed in which the source-/drain-side gates are provided with independent built-in voltages to electrostatically dope the source/drain, while the mid gate is provided with varying voltage which controls the opening and closing of the channel conduction. In order to strengthen the gate electrostatic control over the channel, we adopted double-side gates to sandwich the GNR, as shown in Fig. 1. The thickness of dielectric region is of ∼1 nm with dielectric constant of 5.7 [15], [16]. The channel and electrodes are all made of GNR, avoiding possible formation of Schottky barrier at the channel and electrode interface, which would increase the parasitic contact resistance and deteriorate the device performance. Instead of having armchair GNR (AGNR) of uniform width throughout the whole regions, we employed a semimetal–semiconductor–semimetal sandwiched structure, which is required for designing transistor devices. Concretely, the source, channel, and drain regions are made of semiconductive $3p$ family AGNR (bandgap of ∼1 eV for $3 < p < 10$, according to semiempirical EH method, LDA method, and DFT method), while the electrodes and electrode extensions are made of nearly metallic $3p + 2$ family AGNR (nearly metallic with a bandgap <0.1 eV for $p \geq 3$) [17], [18]. The sub-2-nm-wide edge roughness-free AGNR is used in our simulations. Typically, fabrication of such narrow GNR has proven to be successful, and precise

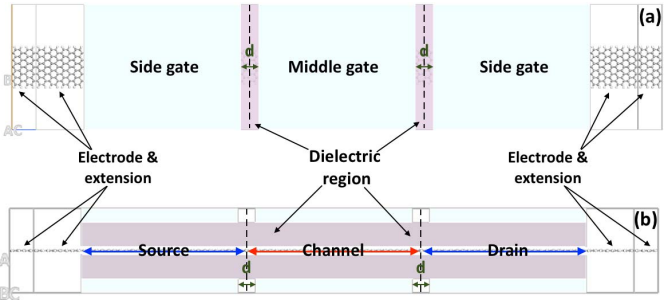

Fig. 1. Schematic of ED-based GNR-TFET. (a) Top view. (b) Side view. AGNR is used, where the AGNR in electrodes and electrode extensions has $3p + 2$ dimmers in the width direction, and AGNR in source, channel, and drain has $3p$ dimmers in the width direction.

control of the line edge roughness is now possible [19], [20]. In order to minimize the geometric difference at the $(3p + 2)$ $-(3p)$ $-$ $(3p + 2)$ AGNR heterojunction interface so that the ribbon-width-mismatch effect on device performance is negligible [3], the same value of p was used for all three regions. Moreover, hydrogen passivation is provided for end atoms on both sides of the GNR which is the most stable thermal configuration for the carbon atoms on the edge.

Prior to simulations, the device geometry is optimized using Tersoff potential [21] until a residual force of 0.001 eV/Å is reached. In order to ensure both accuracy and efficiency, the electronic transport properties of the simulated GNR-TFET device are calculated using semiempirical extended Hückel (EH) method combined with the self-consistent NEGF which are implanted in the Atomistix Toolkit software package [22]–[24]. This approach has been proven to be as accurate as first principles DFT method, but much cheaper computationally. The EH method is suitable for calculating transport properties of carbon-related materials. In EH method, the Hamiltonian is defined as follows:

$$H_{ij} = \begin{cases} E_i + \delta V_H(\vec{R}_i) & \text{if } i = j \\ \dfrac{1}{4}(\beta_i + \beta_j)(E_i + E_j)S_{ij} & \\ \quad + \dfrac{1}{2}[\delta V_H(\vec{R}_i) + \delta V_H(\vec{R}_j)] & \text{if } i \neq j \end{cases} \tag{1}$$

where E_i is an orbital energy and β_i is an adjustable parameter (often chosen to be 1.75). $\delta V_H\left(\vec{R}_i\right)$ is the Hartree potential. S_{ij} is the overlap matrix. In the NEGF, the retarded Green's function is given by

$$G(E) = \frac{1}{(E + i\delta_+)S - H - \Sigma^L(E) - \Sigma^R(E)} \tag{2}$$

where δ_+ is an infinitesimal positive number, and S and H are the overlap and Hamiltonian matrices, respectively. Σ^L and Σ^R are the left and right electrode energy, respectively. When the retarded Green's function is calculated, we could obtain the transmission coefficient which is given by

$$T(E) = G(E)\Sigma^L(E)G^\dagger(E)\Sigma^R(E) \tag{3}$$

where $G^\dagger(E)$ is the conjugate of $G(E)$. After the transmission coefficient is obtained, the transport current can be calculated using Landauer–Bütiker formula which is given as

$$I = \frac{e}{h}\int T(E)\left[f\left(\frac{E - \mu_R}{k_B T_R}\right) - f\left(\frac{E - \mu_L}{k_B T_L}\right)\right]dE \tag{4}$$

where e is the electron charge, h is Planck's constant, f is the Fermi distribution function, and $\mu_{L/R}$ and $T_{L/R}$ are chemical potential and temperature of the left/right electrodes, respectively. In order to make sure the self-consistent calculation converges to the global minimums, the tolerance is set as 10^{-5} and the maximum iteration as 200. A k-point mesh of $5 \times 5 \times 500$ is used for k_A, k_B, and k_C, where C is the transport direction. Pulay–Mixer algorithm is used for iteration with a damping factor of 0.01 and history steps being 20. Density mesh cutoff is set as 100 Ha (1 Ha = 27.1 eV) for numerical accuracy. In order to decouple from the periodic boundary condition, a 20-Å -wide vacuum slab is added in the transverse direction.

The devices geometries considered in this paper have channel length shorter than 10 nm. Thus, carrier transport is assumed to be ballistic, and the electron–phonon coupling effect is not considered in the calculations, which would only be prominent for device with channel length greater than 20 nm [25], [26].

III. Results and Discussion

In this section, the scaling behavior of the ED-based GNR-TFET is presented and discussed. First, we studied the influence of the channel width and length. The I_D–V_{MG} characteristics are calculated, in which I_D and V_{MG} denote the drain current and mid-gate voltage, respectively. Second, the effect of the gate-to-gate distance is studied. Then, the scaling behavior of the built-in voltage applied on the two side gates is explored. Finally, the I_D–V_{MG} response at different supply voltage levels as well as the output characteristics I_D–V_D at different mid-gate voltages is analyzed, in which V_D denotes the drain voltage. Beside the I_D–V_{MG} and I_D–V_D characteristics, the transmission spectrum and the projected local density of states (PLDOSs) are also calculated. The PLDOS is the local density of states that is resolved spatially in the transport direction of the channel using color contour. Utilizing the PLDOS, band diagram for different device geometries and voltage cases can be obtained and analyzed.

A. Influence of Channel Dimensions

According to the results of first principles calculations, the band structure of AGNR is largely dependent on its width. Typically, for $3p$ family GNR, the bandgap decreases as the width increases. Thus, choosing appropriate AGNR channel width is of great importance in optimizing the ED-based AGNR-TFET device performance. In order to study the scaling behavior of the channel width, we examined three device geometries with different channel widths, namely, 9, 15, and 21 atoms, which are all $3p$ family semiconductor AGNR. The corresponding electrodes and electrode extensions are 11, 17, and 23 atoms wide, respectively, which are all $3p + 2$ semimetallic family AGNR. For sake of abbreviation, the devices are named as a11–a9, a17–a15, and a23–a21, respectively.

The AGNR with even-number-atom width (i.e., a8–a6) is not considered for application in our GNR-TFET model. As illustrated in Fig. 2, a8 GNR and a6 GNR have no symmetry in the width direction. As a result, dangling atoms are formed at the a8–a6 GNR interface which would make the device

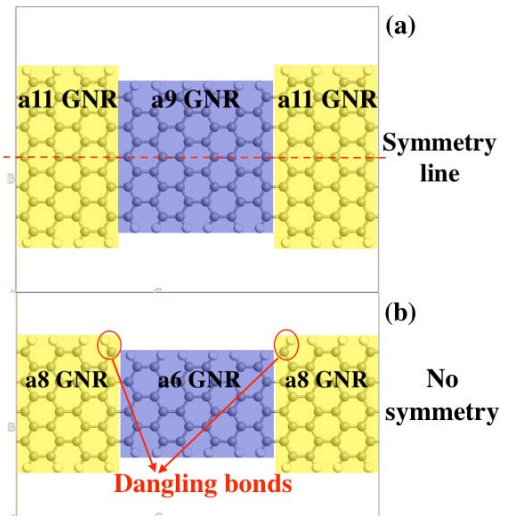

Fig. 2. Illustration of dangling bond formation at a8–a6 heterojunction interface due to lack of symmetry. (a) Geometry of a11–a9 heterojunction. (b) Geometry of a8–a6 heterojunction.

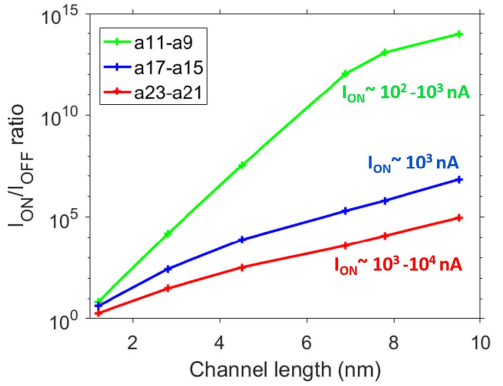

Fig. 3. I_{ON}/I_{OFF} ratio for devices with different widths and lengths, with a fixed supply voltage of 0.2 V and built-in voltage ±3 V for all devices.

structure unstable and deteriorate the performance. It is important to note that the end white atoms on both ends in Fig. 2 are hydrogen passivation atom and, thus, can only have one bond and will not stabilize the shown dangling atom. On the other hand, AGNR with odd-number-atom width has perfect symmetry line in the middle, which gives rise to dangling atom-free structure and is thus considered in our GNR-TFET model. In addition, narrower AGNR structure a5–a3 is not considered in this paper due to its unrealizable narrow width by current GNR fabrication techniques.

As the channel length scales down, the short-channel effect emerges, which severely undermines the gate electrostatic control over the channel and increases the OFF-state leakage current significantly, thus deteriorating the transistor performance. Thus, for each of the three-channel widths studied, the device transfer characteristics are calculated at varying channel lengths from 1.2 to 9.5 nm. For comparison purpose, the supply voltage is fixed at 0.2 V, and the built-in voltage applied on two side gates is ±3 V for all devices. The corresponding I_D–V_{MG} response and the I_{ON}/I_{OFF} ratio are calculated for each case.

Fig. 3 shows the I_{ON}/I_{OFF} ratio for devices with three different channel widths simulated for different channel lengths. The short-channel effect is remarkably observed that as channel

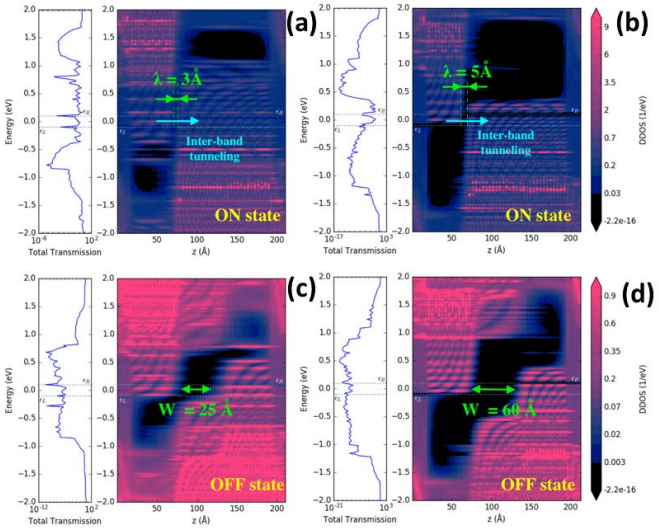

Fig. 4. PLDOS transmission spectrum for two 6.9-nm-long-channel TFET devices with supply voltage 0.2 V and built-in voltage ±3 V on the side gates. (a) and (b) ON-state for a17–a15 and a11–a9 cases. (c) and (d) OFF-state for a17–a15 and a11–a9 cases.

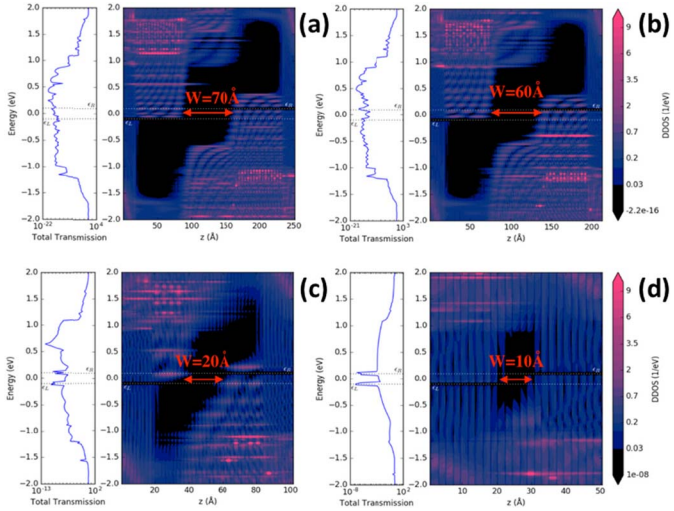

Fig. 5. PLDOSs and transmission spectrum for GNR-TFET device with different channel lengths at OFF-state with supply voltage of 0.2 V and built-in gate voltage of 3 and −3 V for source and drain-side gates, respectively. (a) 7.8 nm. (b) 6.9 nm. (c) 2.8 nm. (d) 1.2 nm.

length decreases the I_{ON}/I_{OFF} ratio decreases exponentially. It is noted that for the a11–a9 case, the short-channel effect is more strongly suppressed as channel length increases.

When $L_{channel} = 9.5$ nm, the I_{ON}/I_{OFF} ratio of a11–a9 case reaches a large value of 10^{14}, while for a17–a15 and a23–a21 cases, smaller values of 10^7 and 10^5 are observed. Thus, in order for our device to have minimum static power consumption at OFF-state while keeping the device size small, the a11–a9 width combination is chosen against the a17–a15 and the a23–a21 geometries.

In order to further analyze the conduction mechanism, the corresponding PLDOS and transmission spectrum are calculated for a17–15 and a11–a9 cases at $L_{channel} = 6.9$ nm.

Fig. 4(a) and (b) shows the ON-state PLDOS of the a17–a15 and the a11–a9 devices. At ON-state, the bandgap in the mid-region shifted upward and the bias window is no longer blocked by the energy barrier, resulting in a large transmission coefficient and high ON-state current. Typically, as the screening tunneling length λ is smaller in the a17–a15 device, its ON-state current is relatively large compared to a11–a9 case. This is also discussed in detail in the next section. In Fig. 4(c) and (d), the OFF-state PLDOS is demonstrated. In order to more clearly identify the energy barrier edge in the middle region, the density of state legend is set as [0–1] $(eV)^{-1}$ instead of [0–10] $(eV)^{-1}$. It is noted in Fig. 4(c) that with smaller bandgap, the a15 GNR also has a narrower energy barrier of 25 Å compared to 60 Å for the a9 GNR shown in Fig. 4(d). Hence, for the a17–a15 device, the direct tunneling between the source and the drain is largely facilitated, and the OFF-state leakage current would increase significantly, resulting in a smaller I_{ON}/I_{OFF} ratio compared to that of a11–a9 at the same channel length.

In order to further analyze the channel length scaling of the a11–a9 device, the OFF-state PLDOS of four different channel lengths is calculated. Fig. 5(a) and (b) shows the OFF-state PLDOS of devices with 7.8- and 6.9-nm channel length, respectively. In both cases, the energy barrier within the bias window (energy range between two dotted white lines) is wide, which are ∼60 and ∼70 Å for 6.9- and 7.8-nm cases, respectively. As a result, the probability for electrons to tunnel through the barrier is negligible, giving rise to a very low OFF-state current of $\sim 10^{-10}$–10^{-11} nA.

Fig. 5(c) and (d) shows the PLDOS for the 2.8- and 1.2-nm channel length cases. It was found that as the channel length becomes shorter, the energy barrier in the bias window becomes narrower, which are ∼20 and ∼10 Å for the 2.8- and 1.2-nm channel length cases, respectively. As a result, the direct tunneling between the source and drain is largely facilitated, and the OFF-state current increases significantly, resulting in an I_{ON}/I_{OFF} ratio of $\sim 10^3$ and $\sim 10^1$, respectively, which are not suitable for any practical applications. As a result, for the a11–a9 device, we choose a tradeoff channel length of 6.9 nm so that the short-channel effect is suppressed while keeping the device size small.

B. Influence of Gate-to-Gate Distance

As discussed in the previous section, the energy barrier width has a major influence on the OFF-state current. When the energy barrier width is greater than 60 Å, the short-channel effect is greatly suppressed. In this section, the gate-to-gate distance is studied. This device geometry parameter is important in determining the energy band profile in the PLDOS and, therefore, affect the device I_{ON}/I_{OFF} ratio.

In Fig. 6(a), two a11–a9 GNR-TFET devices with the same channel length but different gate-to-gate distances are compared. The corresponding I_D–V_{MG} curves are shown in Fig. 6(b). It can be observed that the two curves are similar in shape, and their I_{ON}/I_{OFF} ratio are both $\sim 10^{13}$. However, the I_D–V_{MG} curves for $d = 20$ Å have both lower ON and OFF current. In order to study the conduction mechanism, the PLDOS and the transmission spectrum are calculated for both cases, as shown in Fig. 7.

Fig. 7(a) and (b) shows the ON-state PLDOS for the two cases where the mid gates in both cases are provided with −3-V gate voltage which fully turns the device ON. It can

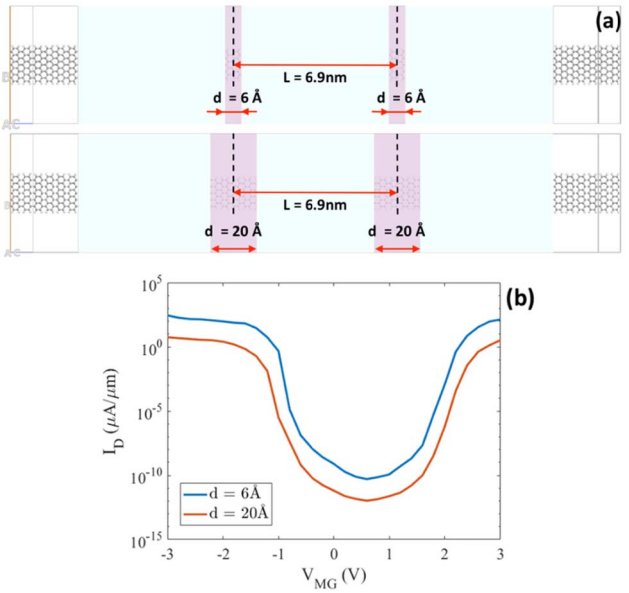

Fig. 6. (a) Device geometries of two GNR-TFETs with different gate-to-gate distances. (b) Corresponding transfer characteristics for the two TFET devices with different gate-to-gate distances.

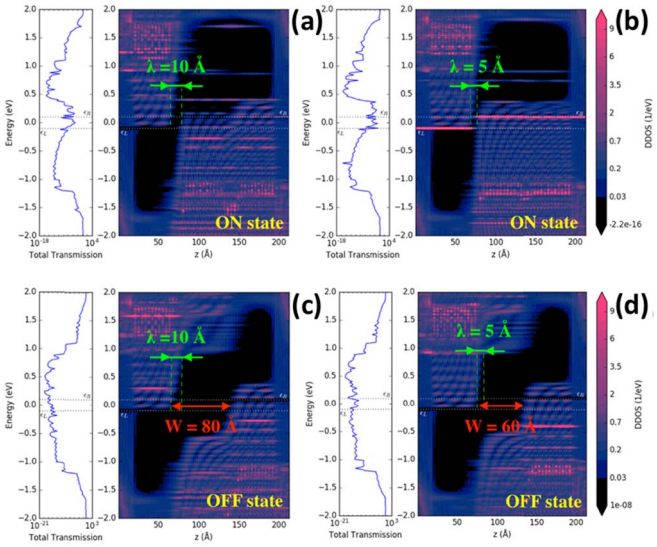

Fig. 7. PLDOS and transmission spectrum of two GNR-TFET device with different gate-to-gate distances with supply voltage 0.2 V and built-in voltage ±3 V on the side gates. (a) and (b) ON-state for the device with larger and smaller gate-to-gate distance, respectively. (c) and (d) OFF-state for the device with larger and smaller gate-to-gate distance, respectively.

be noted that for the device with large gate-to-gate distance, the screening tunneling length λ is also larger, which would result in a smaller transmission probability for the interband tunneling at the ON-state, thus giving rise to a smaller ON-state current. Fig. 8(c) and (d) shows the OFF-state PLDOS for the two cases where the mid gates in both cases are provided with 0.6-V gate voltage. It turns out that as λ increases, the energy barrier width W at OFF-state also increases. As a result, the transmission coefficient in the bias window decreases, leading to a smaller OFF-state current. In summary, although increasing the gate-to-gate distance would cause the ON- and OFF-state current to decrease simultaneously, which leads to little change in the I_{ON}/I_{OFF} ratio, a larger ON-state current

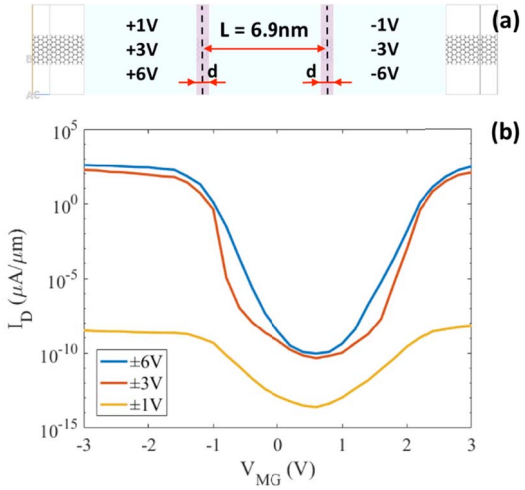

Fig. 8. (a) GNR-TFET device geometry, channel length 6.9 nm, and gate-to-gate distance 6 Å. (b) Transfer characteristics for GNR-TFET with different built-in gate voltages.

is more desirable than reducing the already small enough OFF-state current. Thus, in order to optimize the GNR-TFET performance, it is better to have smaller gate-to-gate distance.

C. Influence of Built-In Voltage on the Side Gates

In order to create an n-i-p junction in the GNR-TFET channel, we use double-side gates to electrostatically dope the source and drain side to be p-type and n-type, respectively. In this section, the scaling behavior of the built-in voltage applied on the side gates is discussed. For comparison purpose, the I_D–V_{MG} characteristics are calculated for GNR-TFET device with three different built-in gate voltages ±1, ±3, and ±6 V, respectively, with all other device parameters kept unchanged.

Fig. 8(a) shows the a11–a9 GNR-TFET device geometry, where the channel length is 6.9 nm and the gate-to-gate distance is 6 Å. The I_D–V_{MG} curves are calculated for each built-in gate voltage as shown in Fig. 8(b). It can be observed that the ±3- and ±6-V cases have comparable ON- and OFF-state current and similar I_D–V_{MG} curves, except that the ±3-V case has wider OFF-state region. For the ±1-V case, however, the I_D–V_{MG} curves are quite different. The ON-state current is much lower than the other two cases, giving rise to much lower I_{ON}/I_{OFF} ratio of 10^5. Again, in order to analyze the conduction and switching mechanism at different built-in gate voltages, the PLDOS and transmission spectrum are calculated for each case.

Fig. 9(a) and (c) shows the ON-state PLDOS for ±6- and ±3-V cases. In both cases, the source and drain-side bandgap regions are shifted downward and upward, respectively, with enough amount of energy, and the bias window [−0.1 eV, 0.1 eV] is not overlapping with any bandgap, resulting in a channel with high tunneling probability inside the bias window and, thus, a high ON-state current of $\sim 10^3$ nA. In Fig. 9(e), for the ON-state PLDOS of ±1-V case, however, the voltage applied on the two side gates does not produce strong enough electric field to shift the source- and drain-side bandgap regions far away from bias window; therefore, the bias window is inside the bandgap region. As a result, the conduction

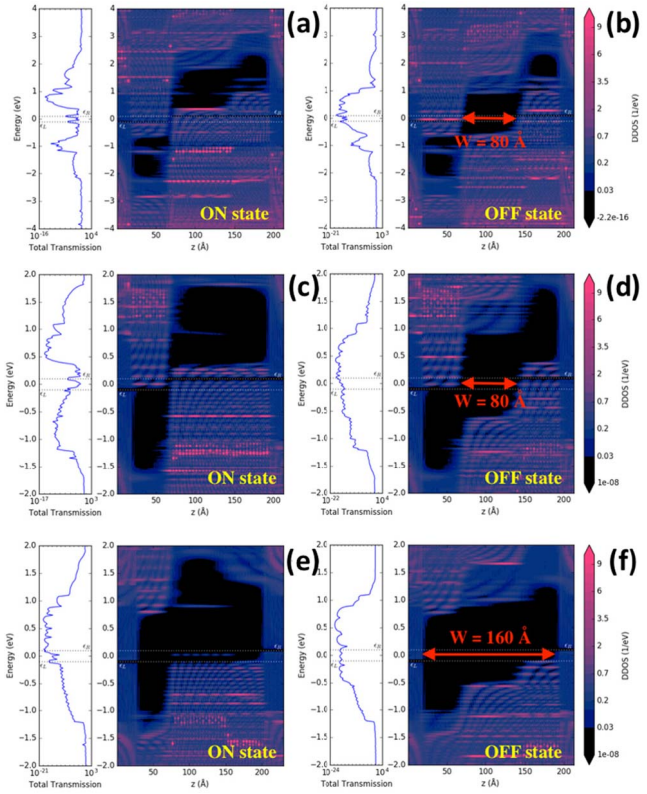

Fig. 9. PLDOS and transmission spectrum for GNR-TFET device under different built-in gate voltages with supply voltage of 0.2 V. (a), (c), and (e) ON-state PLDOS and transmission spectrum for the GNR-TFET under ±6-, ±3-, and ±1-V built-in gate voltage, respectively. (b), (d), and (f) OFF-state PLDOS and transmission spectrum for the GNR-TFET under ±6-, ±3-, and ±1-V built-in gate voltage.

channel is still blocked even at the ON-state, giving rise to a very low ON-state current of $\sim 10^{-9}$ nA. Similarly, as shown in Fig. 9(f), because the source- and drain-side bandgaps overlap with the bias window, the energy barrier width W is largely widened; thus, the OFF-state current for ±1-V case is also much lower compared with the ±3- and ±6-V cases.

In summary, in order for ED-based GNR-TFET to have strong switching feature with high ON-state current, the channel must be fully open at the ON-state without being blocked by any energy barrier. This is achieved when the source- and drain-side bandgaps have an energy difference greater than $E_g + eV_b$, where E_g is the bandgap, V_b is the supply voltage, and eV_b is the bias window range. Thus, the built-in gate voltage must be high enough that the source and drain sides of the channel could be sufficiently doped, and therefore, the source- and drain-side bandgap could shift far away from the bias window.

D. Influence of Drain Voltage

In the conventional MOSFET, the drain voltage is important in determining the I_D–V_G characteristics [5]. Typically, the minimum OFF-state current I_{min} is reached at $V_G = 1/2V_D$ where V_D is the drain voltage. In addition, as V_D increases, the I_{min} increases exponentially, which lead to a potential issue of high leakage current. In this section, we study the scaling effect of the supply voltage on the I_D–V_{MG} curves of the a11–a9 ED-based GNR-TFET. Five drain voltage values

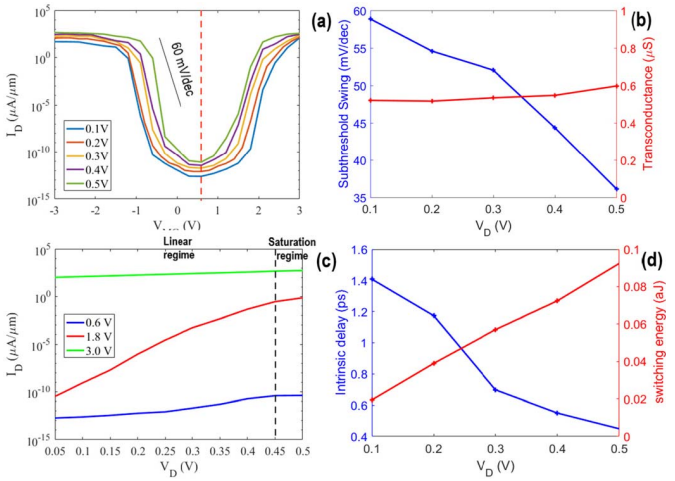

Fig. 10. (a) Transfer characteristics under different drain voltages. (b) SS and transconductance under different drain voltages. (c) Output characteristics at different mid-gate voltages. (d) Intrinsic delay and switching energy under different drain voltages.

ranging from 0.1 to 0.5 V are examined. The device geometries are the same as in the last section, as shown in Fig. 8(a).

Fig. 10(a) shows that both the ON- and OFF-state currents at all V_D have a comparable magnitude, resulting in a large I_{ON}/I_{OFF} ratio of $\sim 10^{14}$. Unlike MOSFET, the transfer characteristics for ED-based GNR-TFET are immune to V_D change in that I_{min} does not increase as V_D increases, and the corresponding V_{MG} of I_{min} does not shift as V_D changes. This feature would enable the ED-based GNR-TFET to be more commonly used at different working conditions without specific gate work function engineering. In addition, it was noted in the left axis of Fig. 10(b) that the SS decreases as V_D increases and at $V_D = 0.5$ V, a smallest SS of 35 mv/decade is reached. The scalable SS below 60 mv/decade of the ED-based GNR-TFET shows promising potential for designing low-power consumption transistor. Meanwhile, the transconductance (g_m) which equals to $\partial I_D/\partial V_{MG}$ is calculated at the threshold V_{MG} under a different V_D as shown in the right axis of Fig. 10(b). It is noted that g_m has an average value of 0.55 μs and is nearly invariant to V_D change.

Apart from the transfer characteristics, the output characteristics I_D–V_D are also reported for three different mid-gate voltages, namely, 0.6, 1.8, and 3.0 V, which corresponding to the OFF-state, the threshold state, and the ON-state. Typical linear and saturation regimes can be observed on Fig. 10(b). It is noted that the slope of the linear regime is larger at the threshold state of $V_{MG} = 1.8$ V than that at the OFF-state of $V_{MG} = 0.6$ V and ON-state of $V_{MG} = 3.0$ V. This is also an indicator of smaller SS at higher drain voltage.

In addition, the dynamic performance of the device is evaluated at a different V_D. Fig. 10(d) shows that the intrinsic delay (D_{ini}) which equals to $(Q_{ON} - Q_{OFF})/I_{ON}$ decreases as V_D increases, while the switching energy (E_{sw}) which equals to $(Q_{ON} - Q_{OFF}) \times V_D$ increases as V_D increases, where Q_{ON} and Q_{OFF} are the ON-state and OFF-state channel charges, respectively. Fig. 10(d) shows that D_{ini} and E_{sw} have small values of ~1 ps and ~0.05 aJ, compared to the requirement in the ITRS 2030, showing its promising potential for radio frequency application.

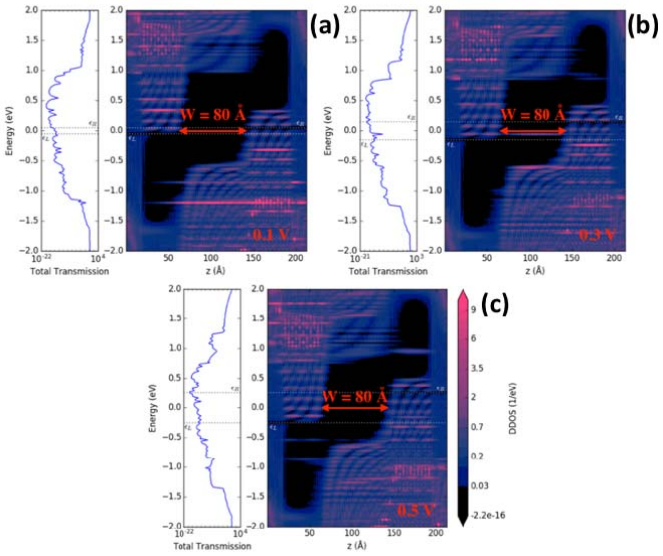

Fig. 11. OFF-state PLDOS and transmission spectrum at different supply voltages. (a) 0.1 V. (b) 0.3 V. (c) 0.5 V.

In order to analyze the transfer characteristics at different V_D, the PLDOS and transmission spectrum are calculated, as shown in Fig. 11. It is noted that as V_D increases the source- and drain-side bandgaps move downward and upward, respectively, by eV_D, which guarantee that at the source and drain sides, the bias window is always outside any bandgap, enabling the channel to be always fully open at the ON-state. Thus, ON-state current at different supply voltage levels has the same magnitude. Meanwhile, the bandgap position and the mid region do not change with V_D and the energy barrier width W is the same in all cases. Thus, the OFF-state current at different V_D also has comparable magnitude. In addition, due to different work functions of the metal gate and the AGNR electrode, the CB and the VB at the mid region are not symmetric about 0 eV at OFF-state. Therefore, I_{min} is reached at some positive gate voltage close to 0.6 V instead at 0 V.

IV. Conclusion

We studied optimizations of an ED-based AGNR-TFET device. Using EH semiempirical method combined with self-consistent NEGF, we performed a comprehensive simulation study on the device scaling behavior. The current–gate voltage characteristics are calculated. An I_{ON}/I_{OFF} ratio as $\sim 10^3$ μA/μm. A sub-60 mv/decade SS was observed (35 mv/decade). Through the discussion of channel length and width, gate-to-gate distance, built-in gate voltage, as well as the supply voltage, we propose a design guideline for ED-based GNR-TFET performance optimization summarized as follows.

1) The a11–a9 channel geometry has strongest suppression on the short channel effect, and thus it is preferred for low-power applications.
2) To suppress short channel effect while keeping the device size small, a tradeoff channel length 6.9 nm is chosen for the a11–a9 device.
3) Smaller gate-to-gate distance in the order of 6 Å facilitates a larger ON state current.
4) In order for a device to have strong switching feature, the built-in gate voltage must be large enough to produce an energy differential ΔE greater than $E_g + eVb$ for source and drain-side band gap.
5) The I_D–V_{MG} characteristic of ED-based GNR-TFET is immune to V_D change. The subthreshold swing is scalable with V_D.

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