Spin Qubit Device Integration

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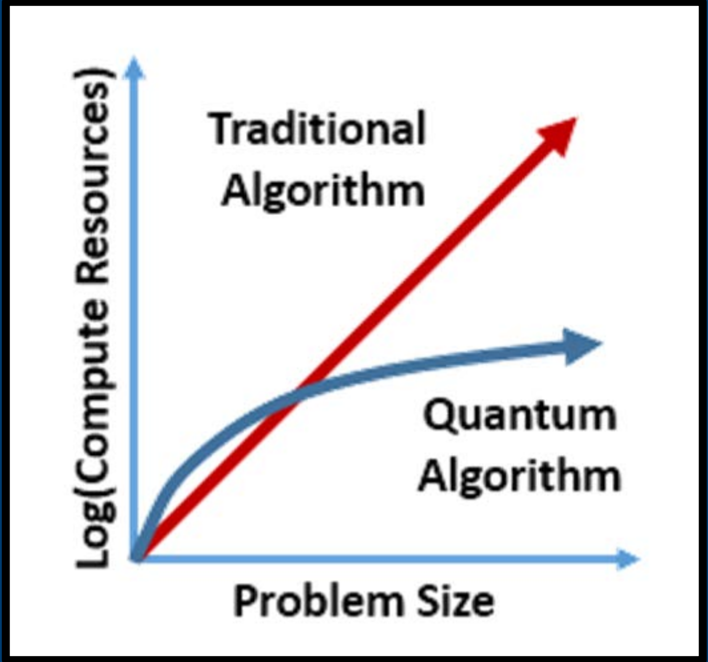
Intel is Leveraging Transistors for Spin Qubits, but there are 3 Key Challenges:

- New 300mm process innovations specific for qubits
- High volume electrical characterization
- Interconnects and array scalability

The Promise of Quantum Computing

TIME “Quantum Will Change Everything”



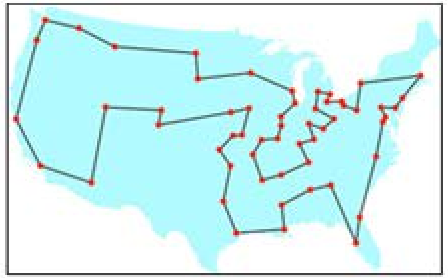
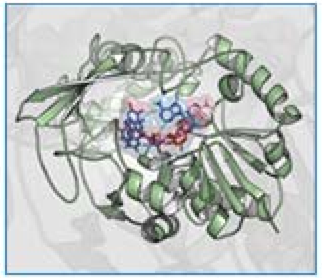
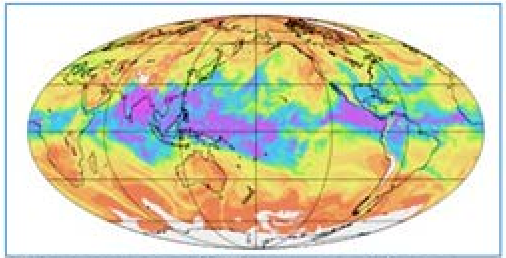

Travel and Logistics


Image Processing


Pharmacology


Improved Forecasting


Improved Stock ROI

Cryptography

Potential to provide an exponential speedup in compute for certain applications

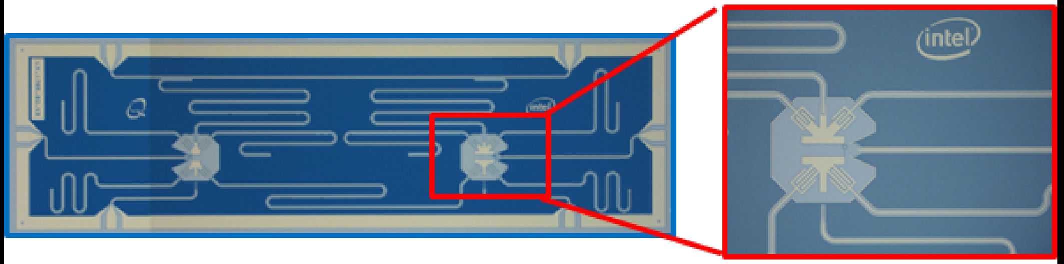
Quantum Computing at Intel

- Quantum Algorithms
- Quantum Software
- Quantum Architecture
- CMOS/CRYO – Control logic
- Interconnects / package
- Devices / Qubits
- Materials

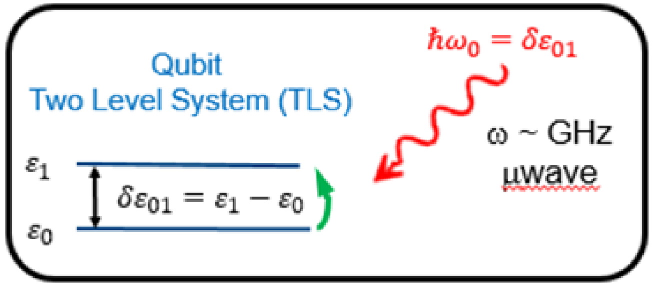
More interested in a scalable system, rather than a brute force 50 qubit milestone

Building Better Qubits

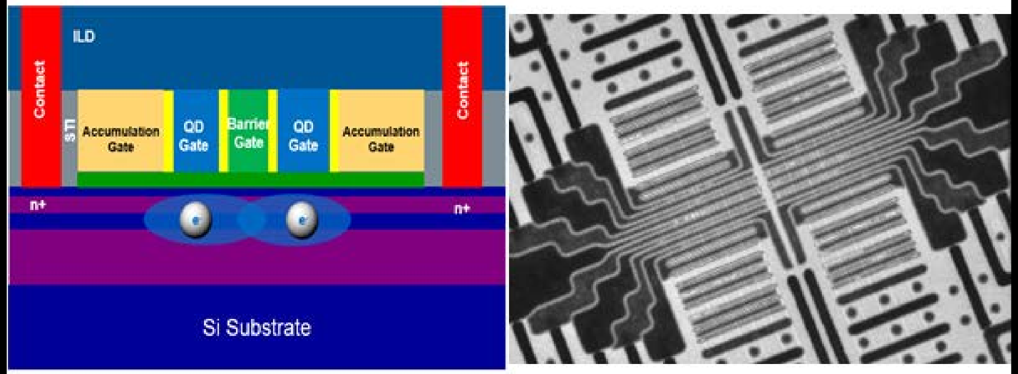
Superconducting Qubits



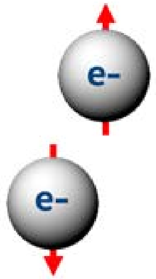
Very high quality microwave circuit



Spin Qubits in Silicon

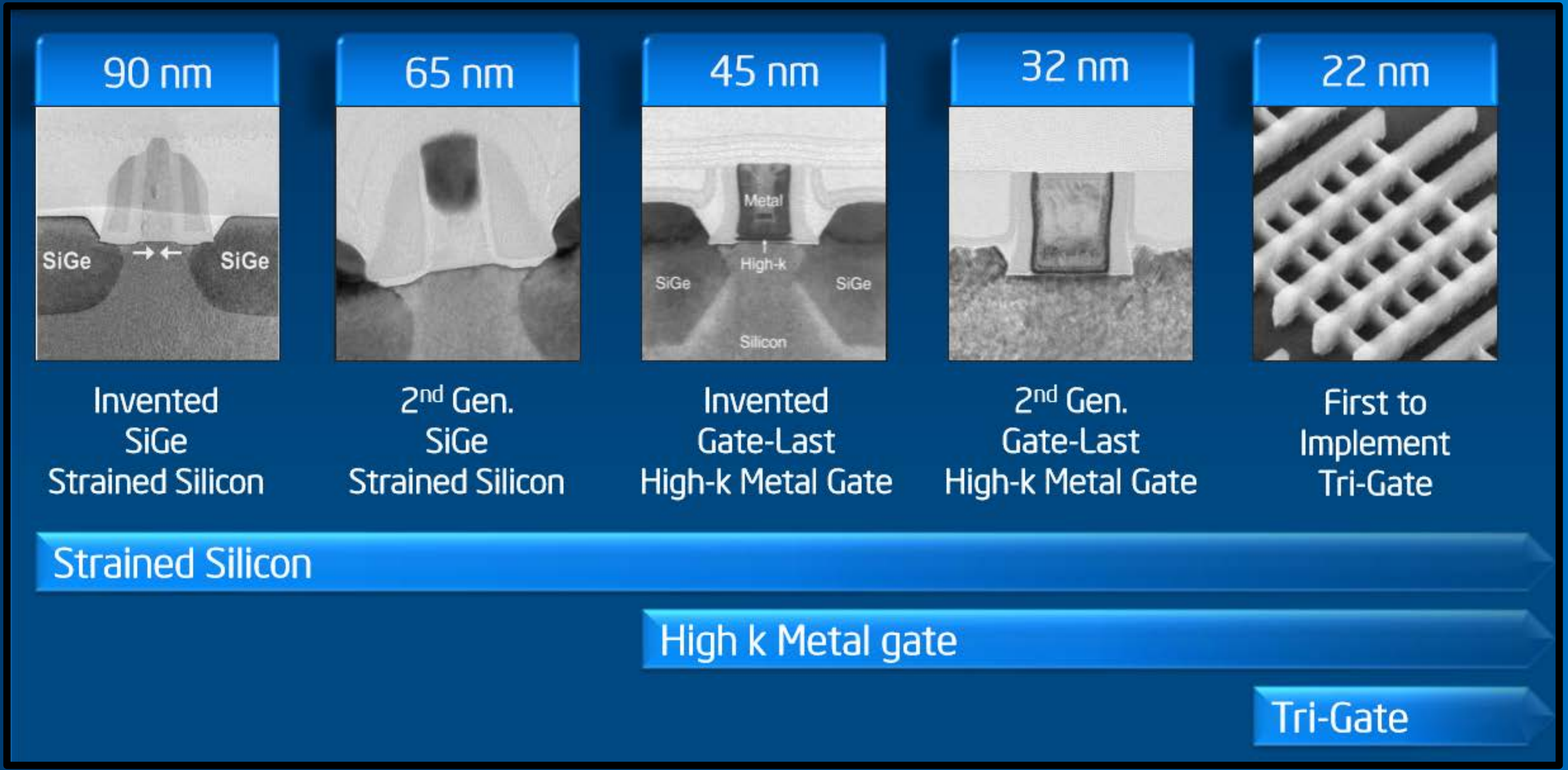


Single electron transistors, where qubit is spin state



Intel is investigating superconducting (interconnect like) and spin (transistor like) qubits

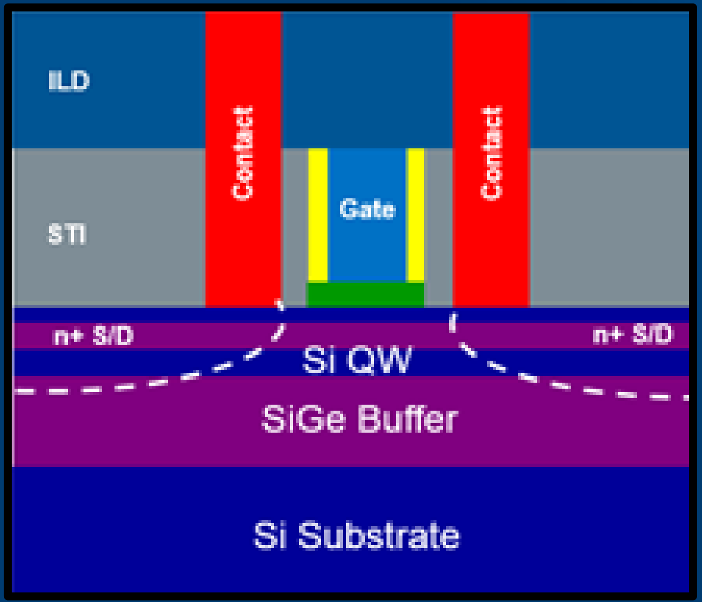
Intel Transistor Leadership



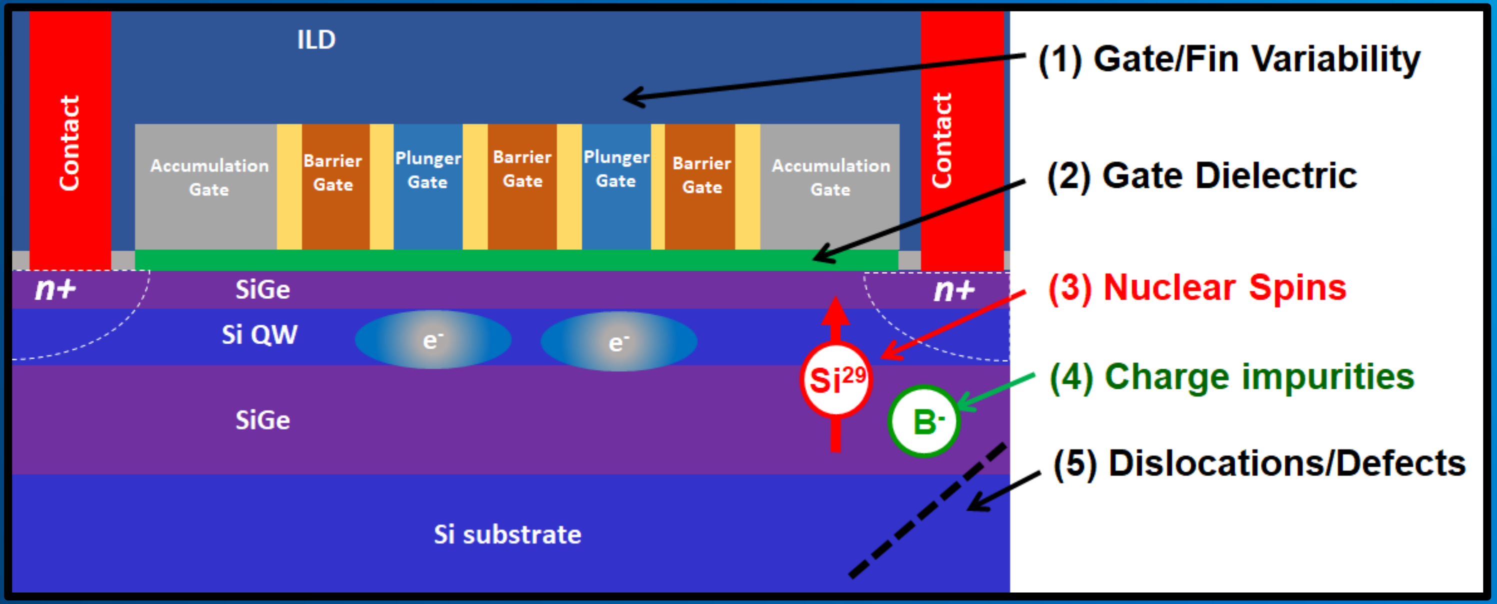
Leverage 300mm high volume fabrication + characterization expertise in transistors towards spin qubits

From Transistors to Quantum Dots

Transistor



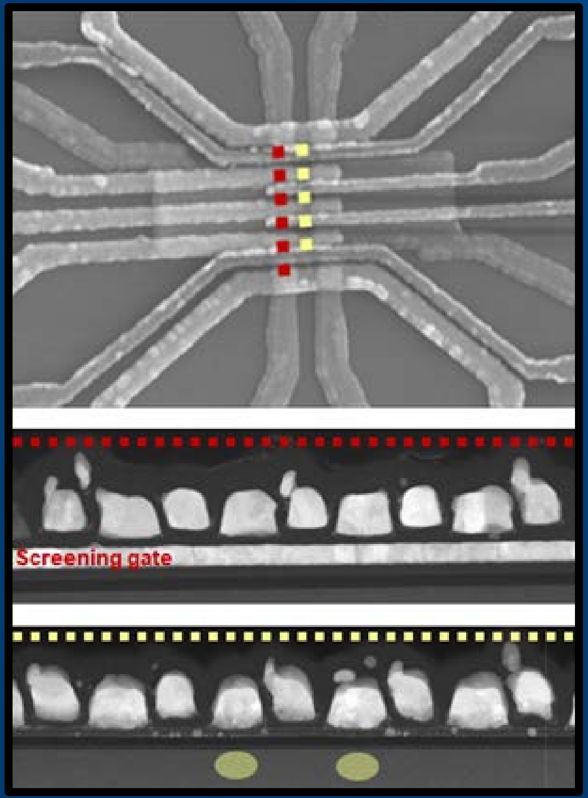
Quantum Dot Device



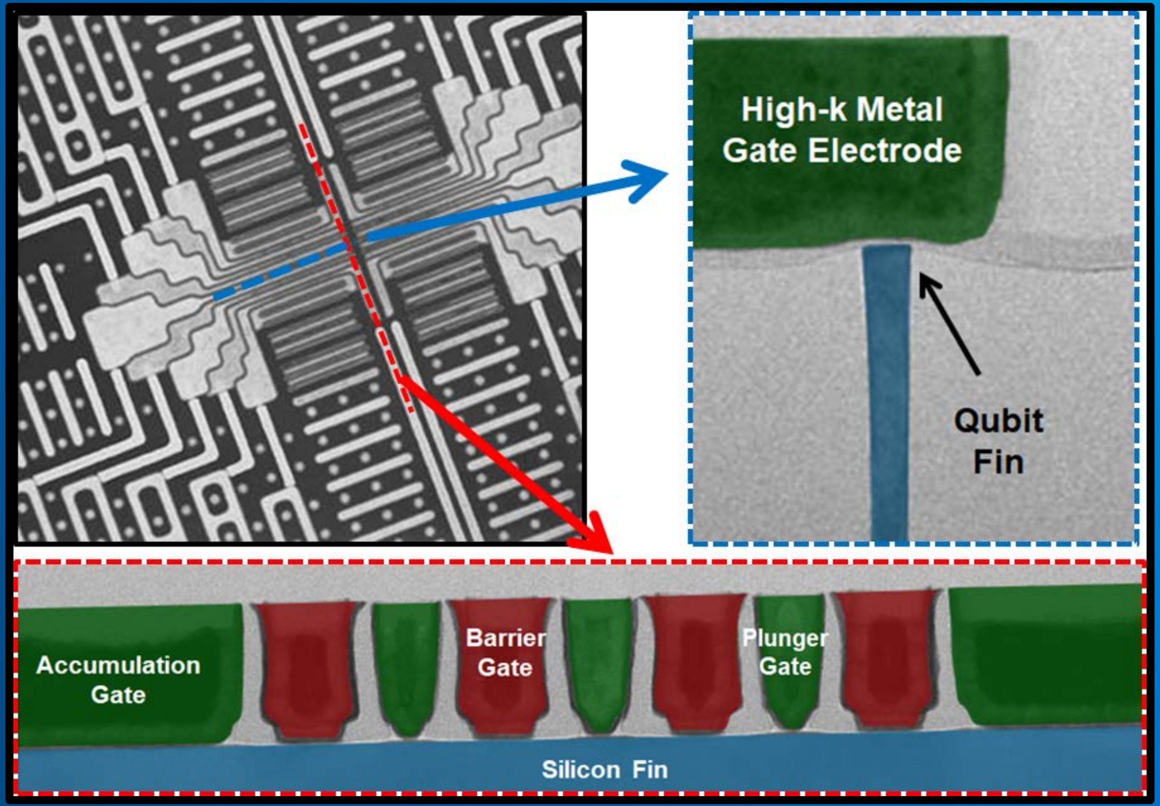
Quantum dots are very similar to transistors and face many of the same process challenges

Challenges moving to a 300mm Qubit Flow

Academic Device

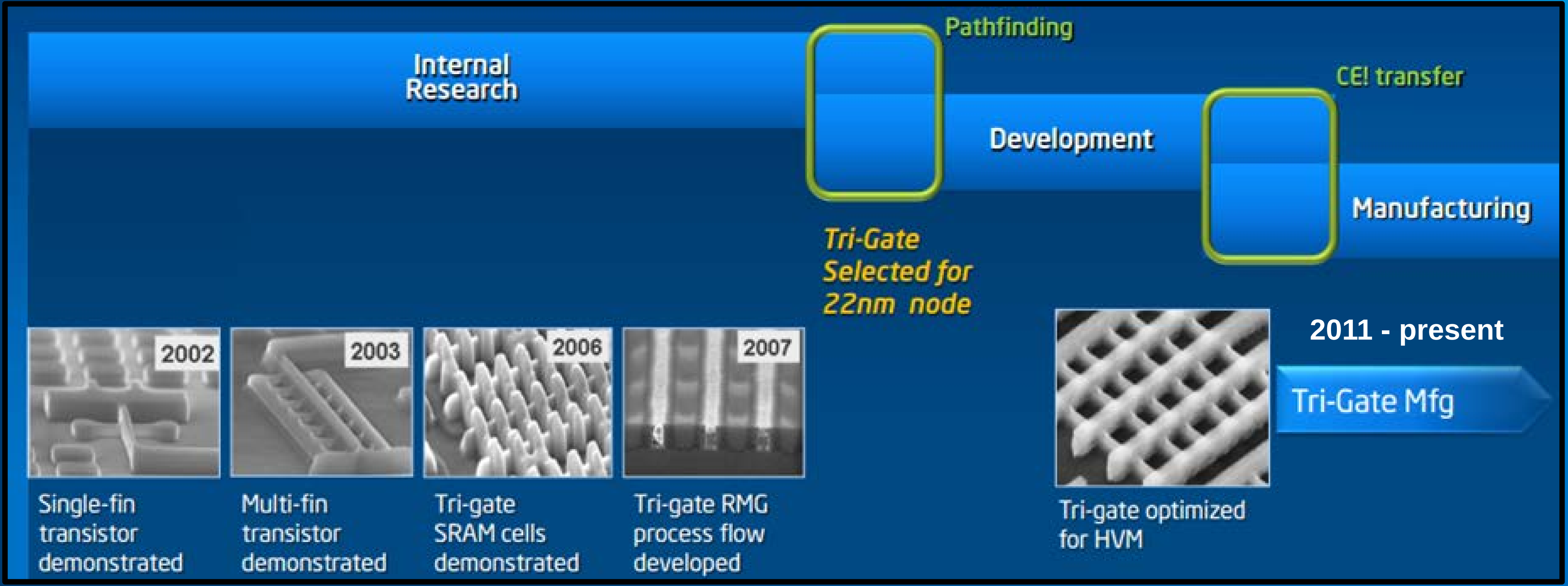


Intel 300mm Device



- **Lift-off based academic devices never see standard plasma etches and polish steps used in 300mm**
- **Academic devices are fully electrostatically defined (no silicon etch) and use thick thermal SiO2 ; current state-of-art 300mm transistor process uses etched STR Fins and scaled high-k gate oxide**

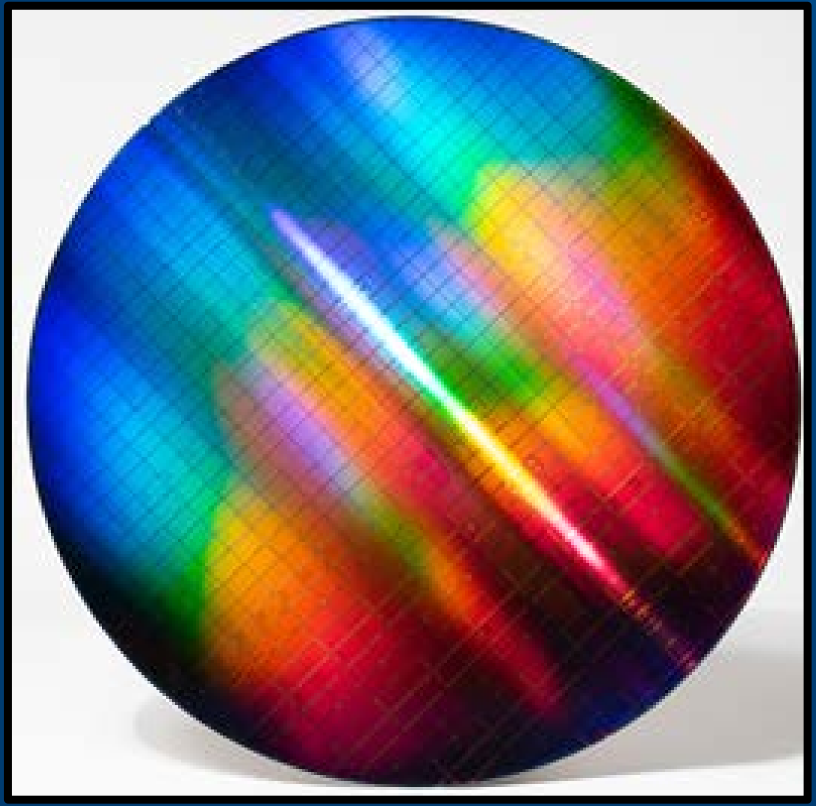
Trigate Transistor R+D Timeline



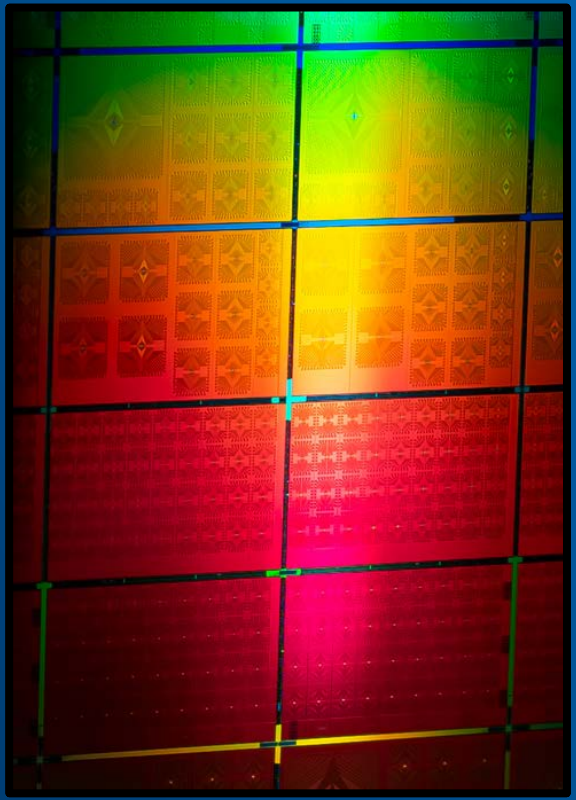
Nine years from initial 300mm research to manufacturing

Customized Testchip for Spin Qubits

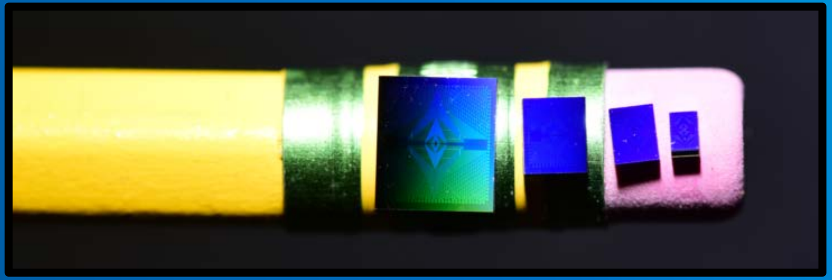
Full 300mm Wafer



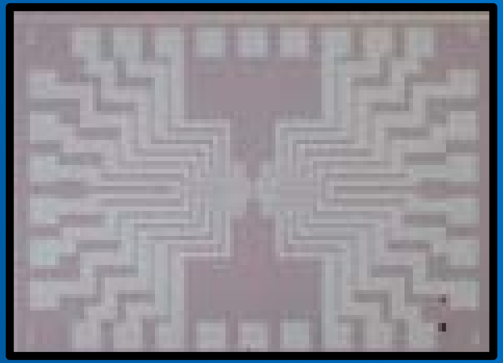
Full Reticle



Individually diced 55, 23, 15, and 7 gate arrays

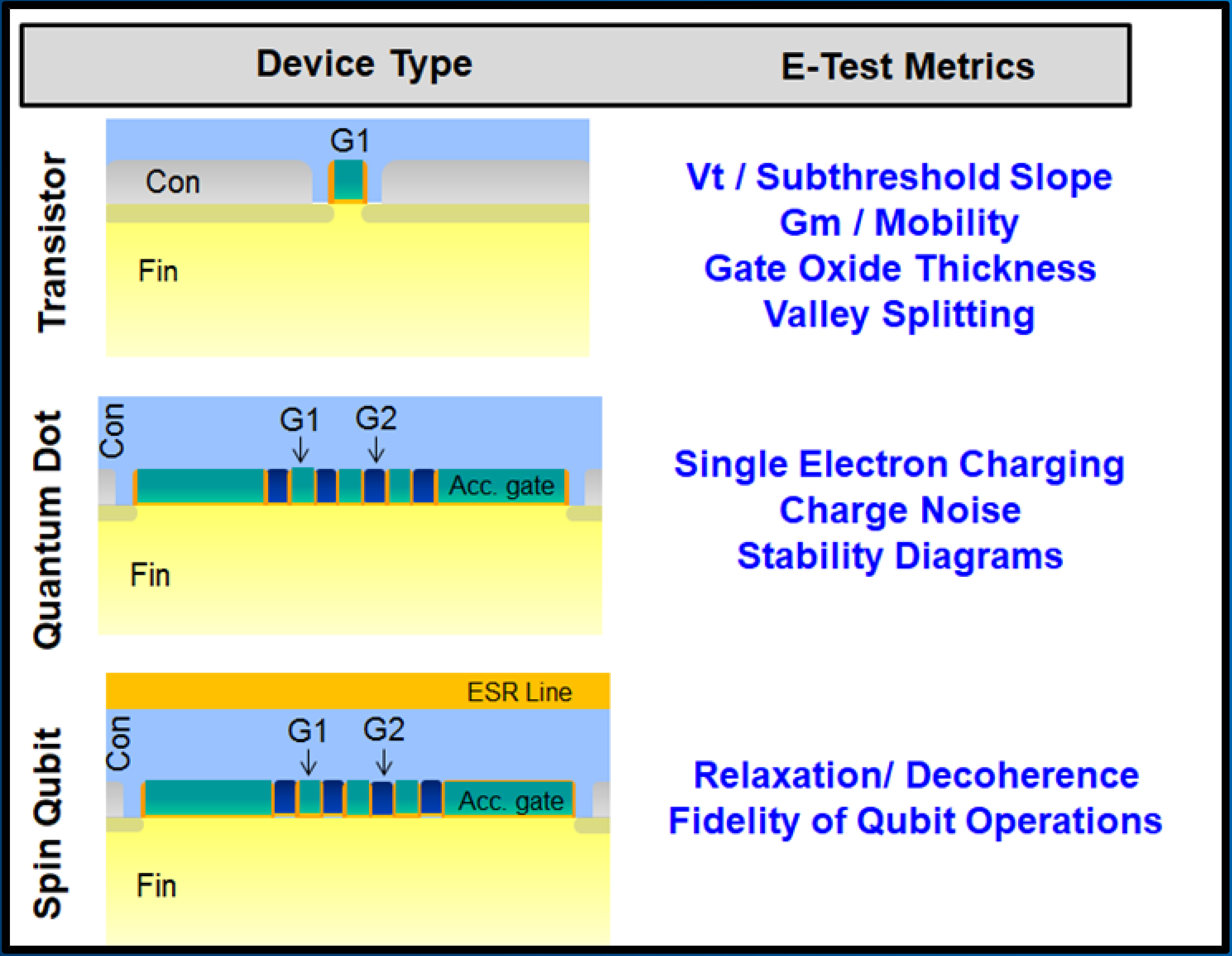


7 gate array

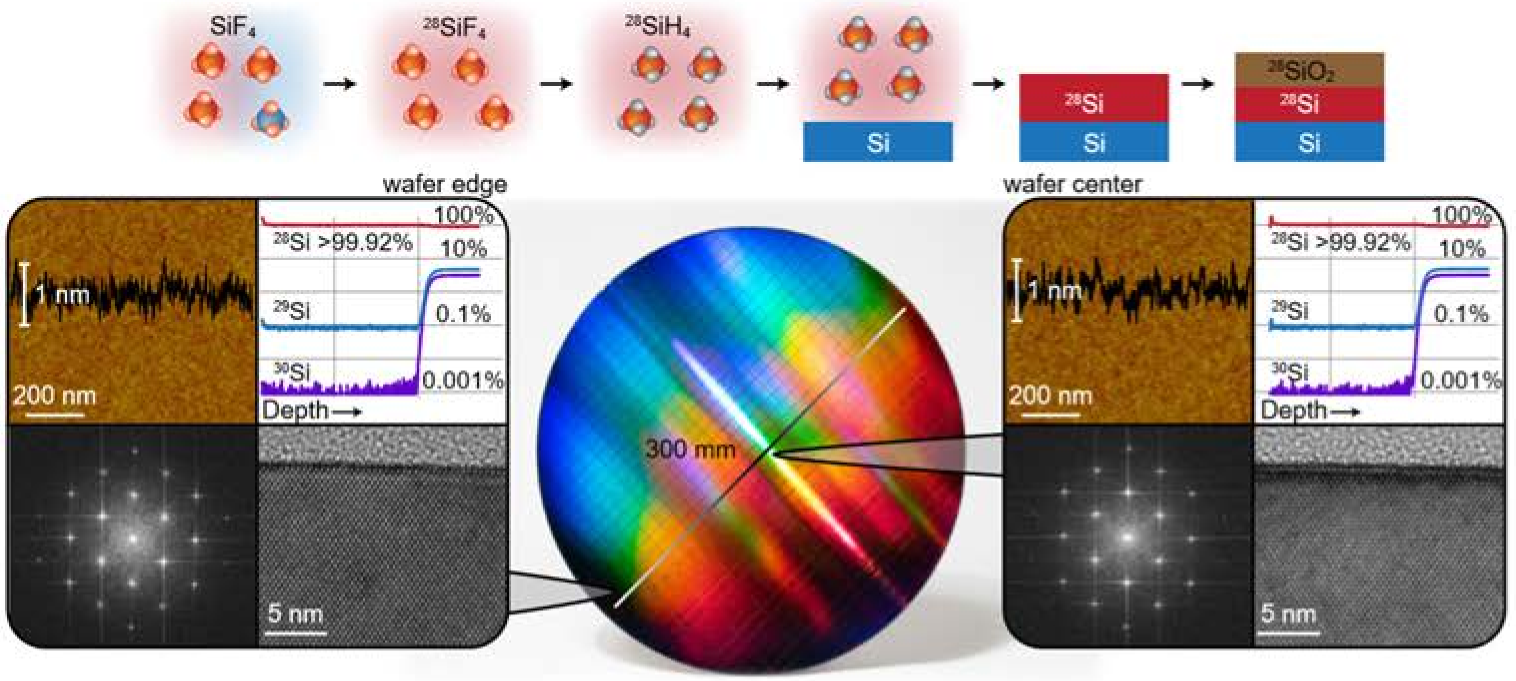


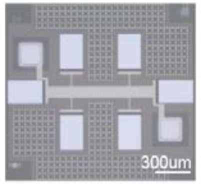
Enables 300mm device integration line for spin qubits, with each wafer having over 10,000 qubit testrows

Transistors → Quantum Dots → Qubits

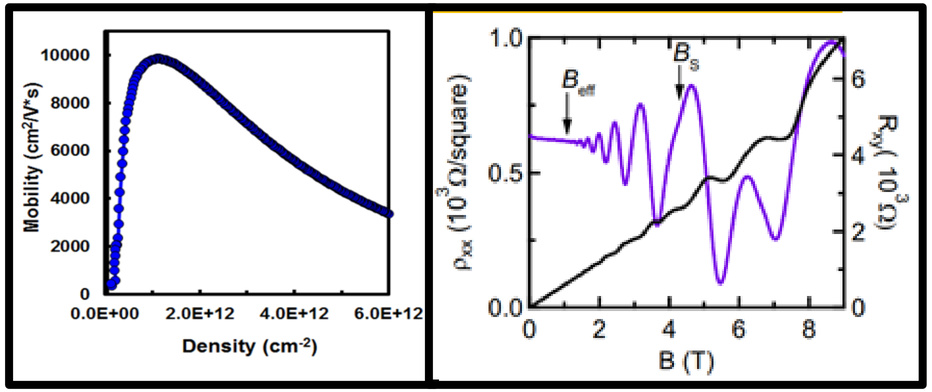


^{28}Si 300mm Substrate Development





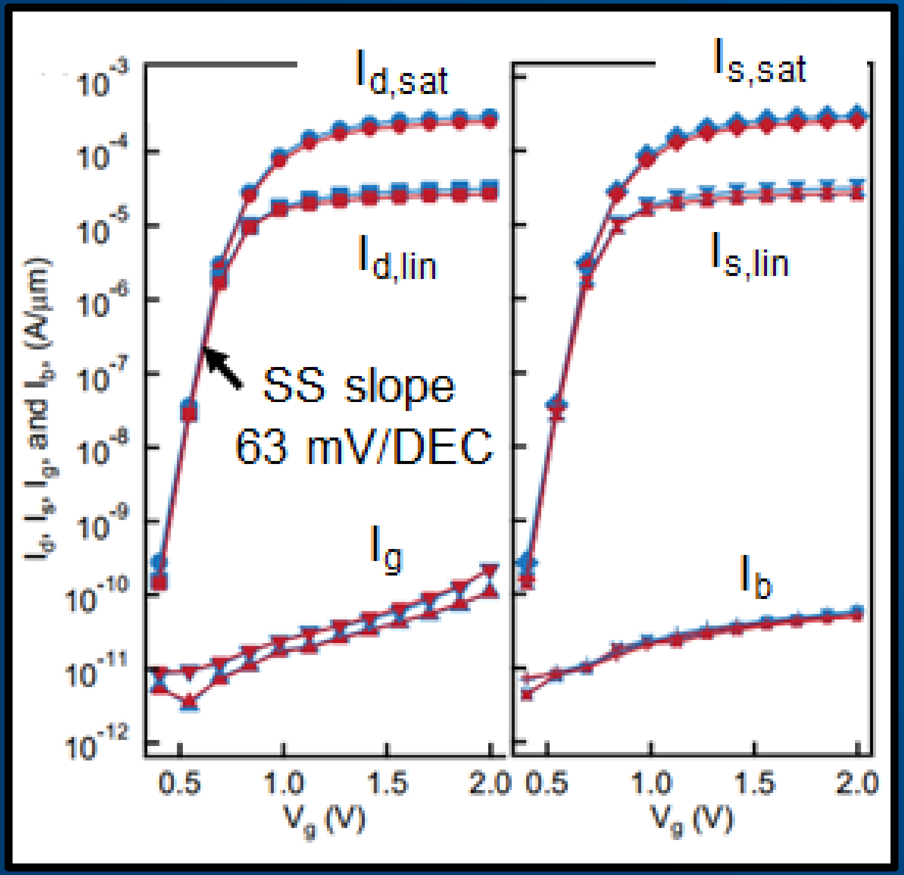
Hall mobility of 10,000 is highest reported for this oxide thickness (17nm)



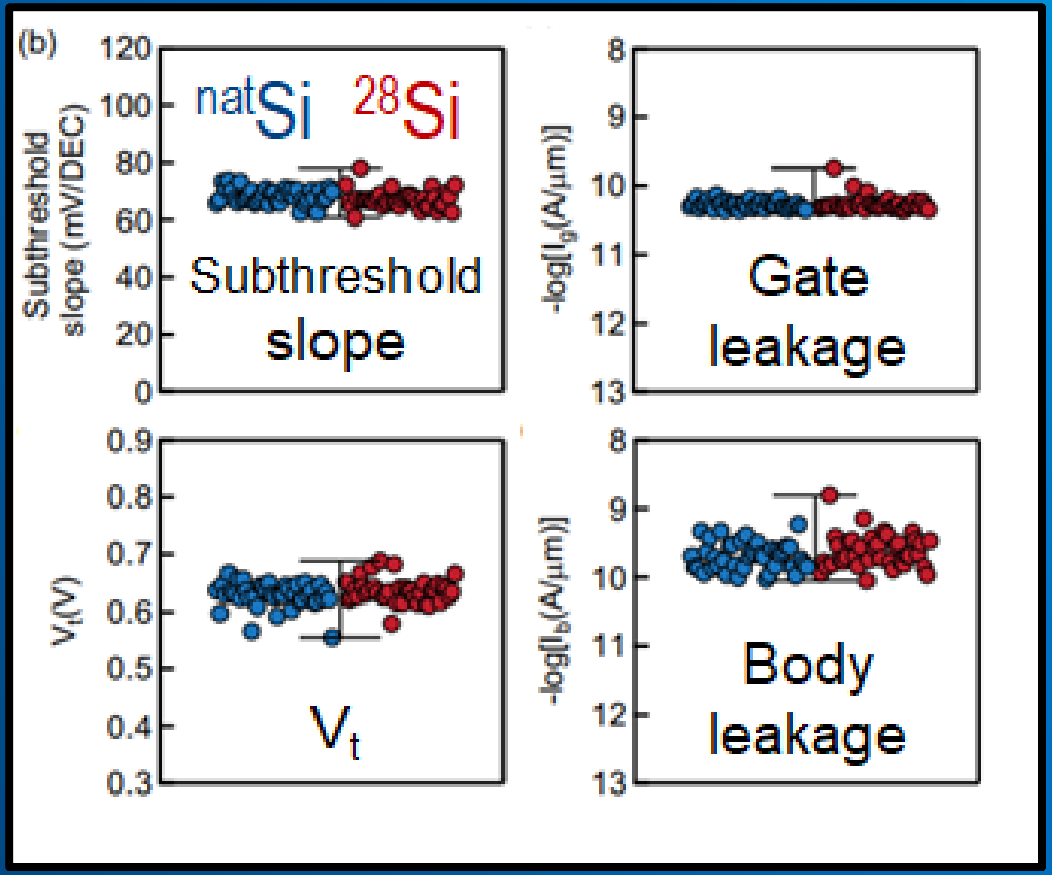
Created ecosystem for high quality / high volume substrates for Quantum Computing research

^{28}Si and Natural Si Transistor Data Matched

Typical Devices



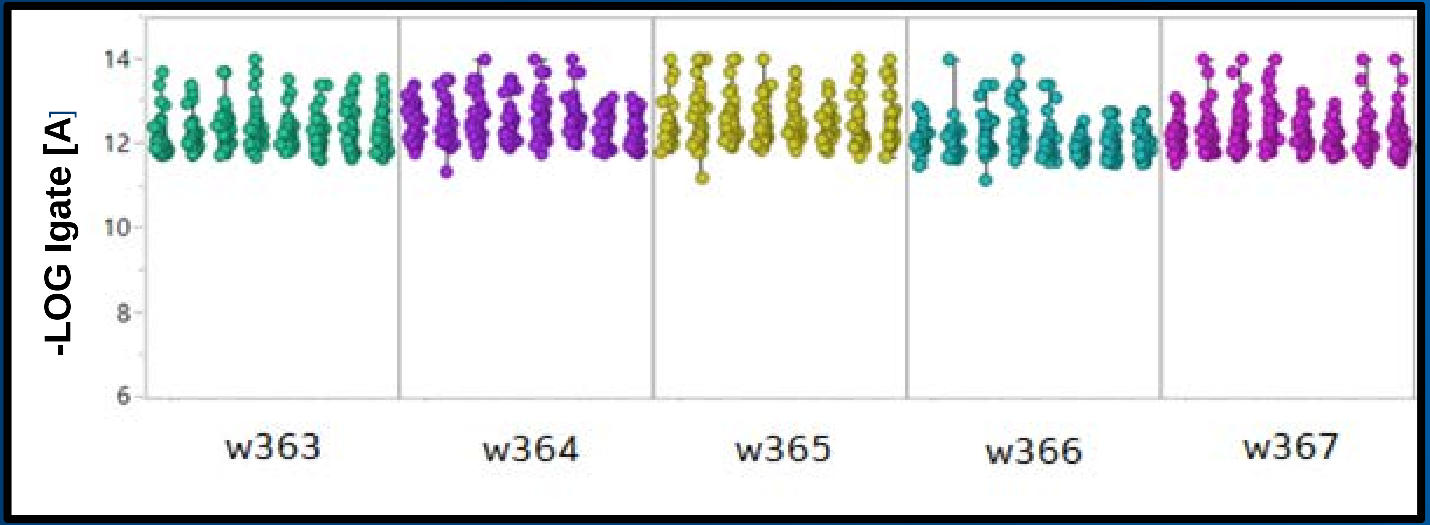
Cross Wafer Distributions

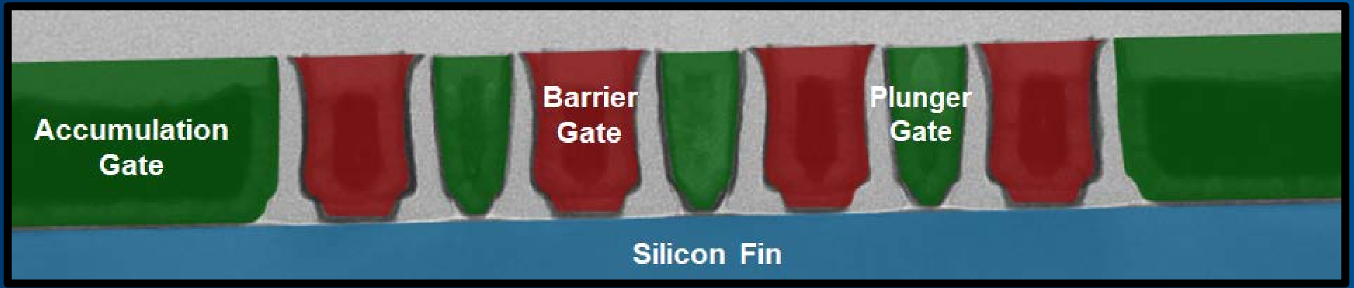


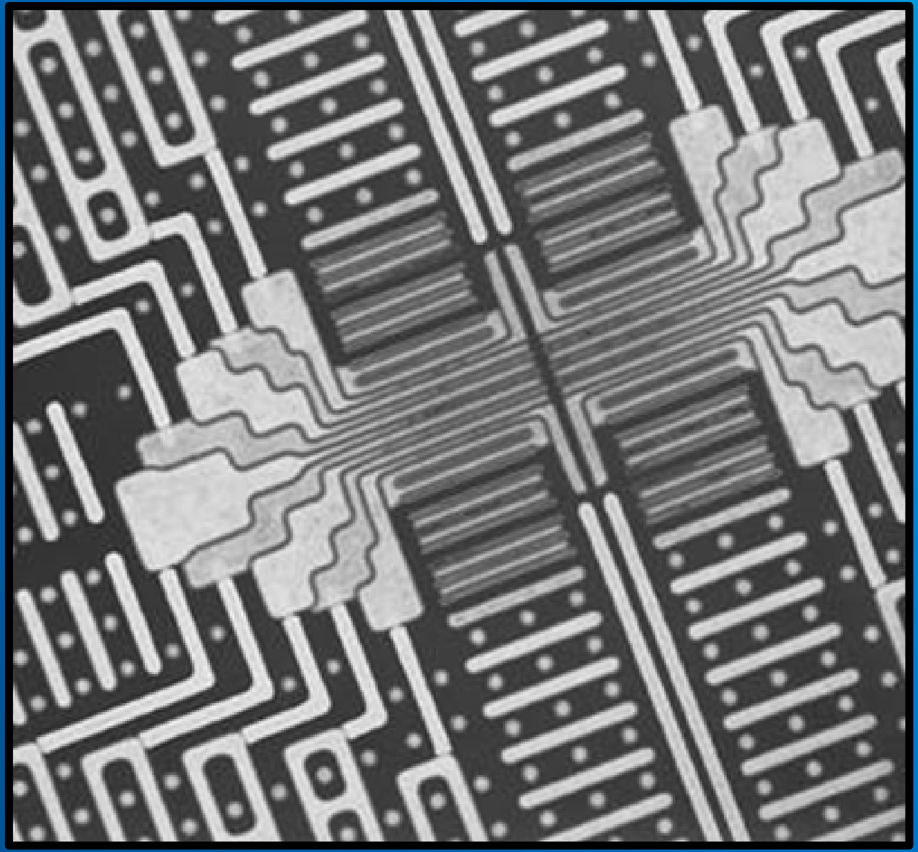
^{28}Si and ^{Nat}Si process identically though the fab

Quantum Dot Gate Yield is virtually 100%

Gate leakage from individual barrier, plunger and accumulation gates across the wafer

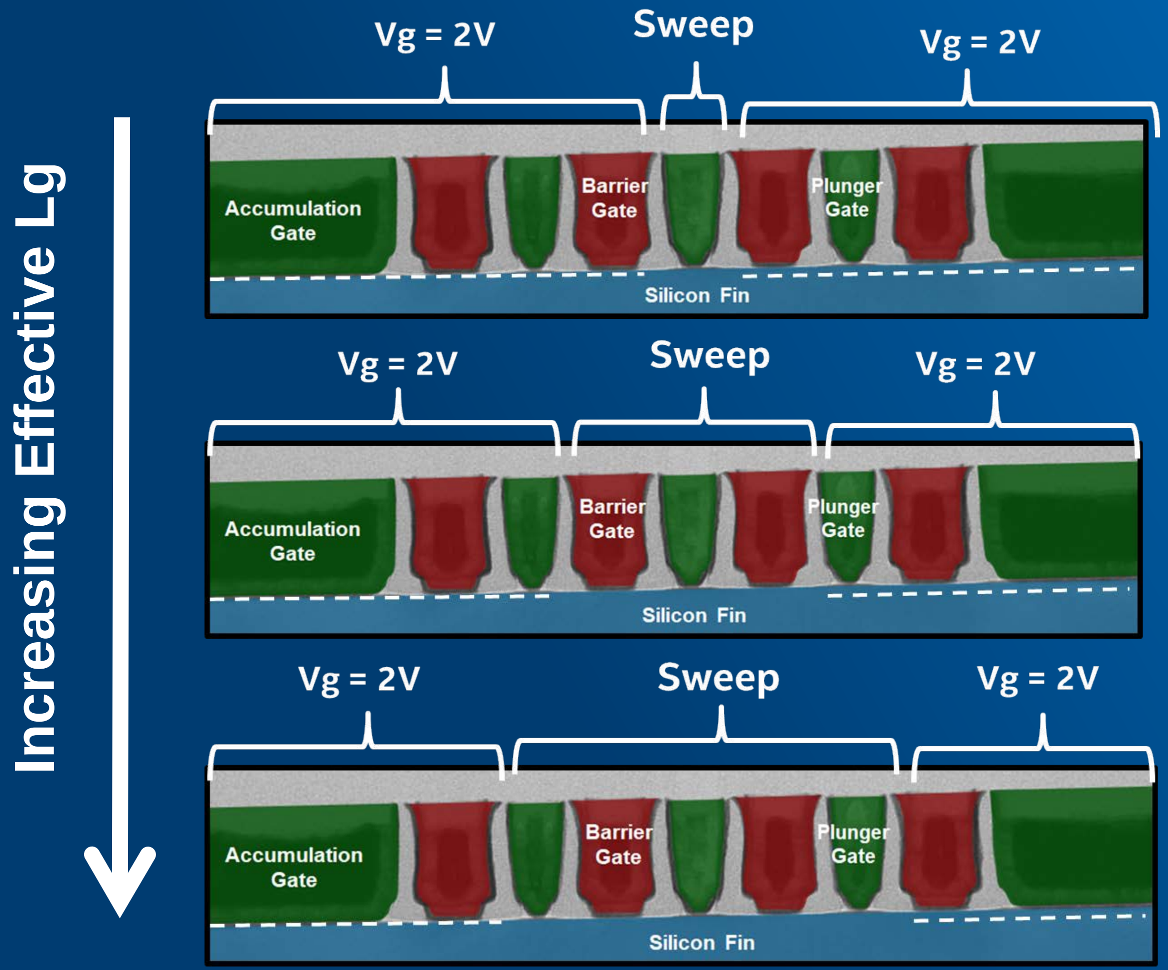


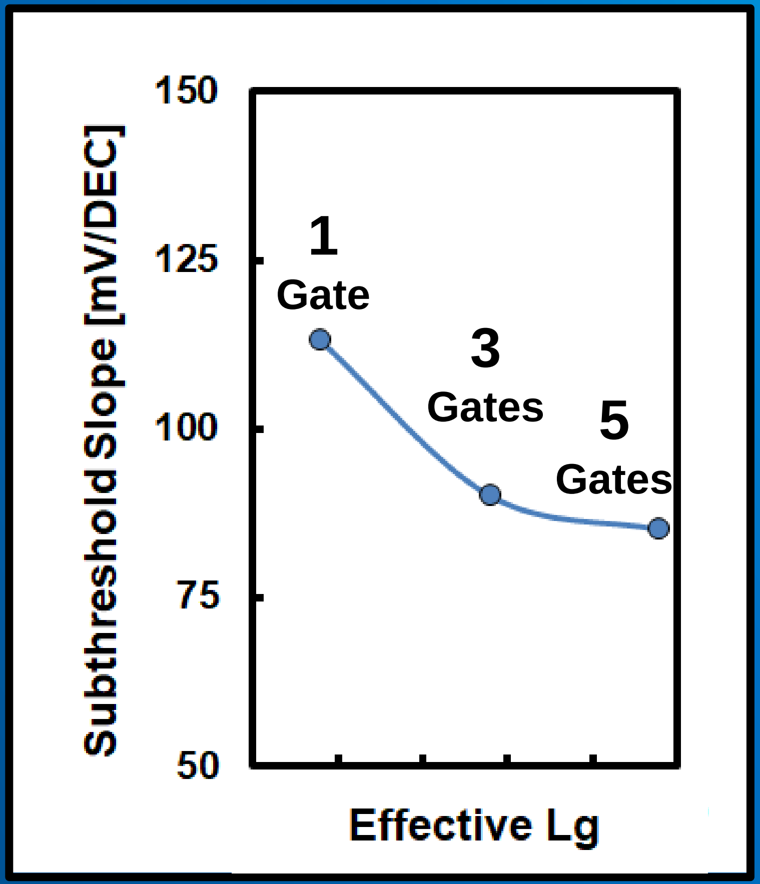




Compared to coupon line this enables statistical data collection and scaling up to larger arrays

Transistor Metrics to Characterize Gate Interface

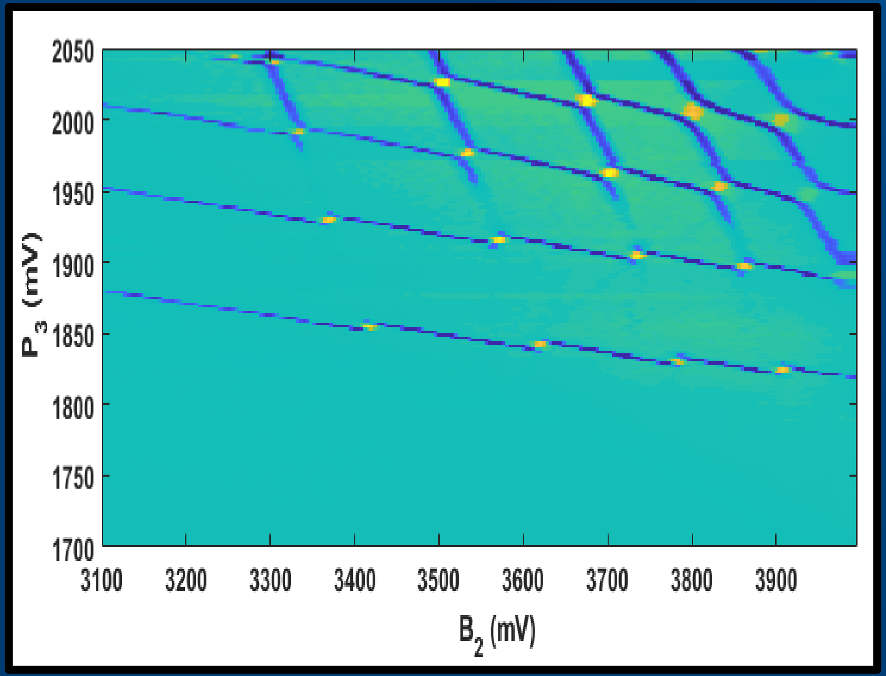




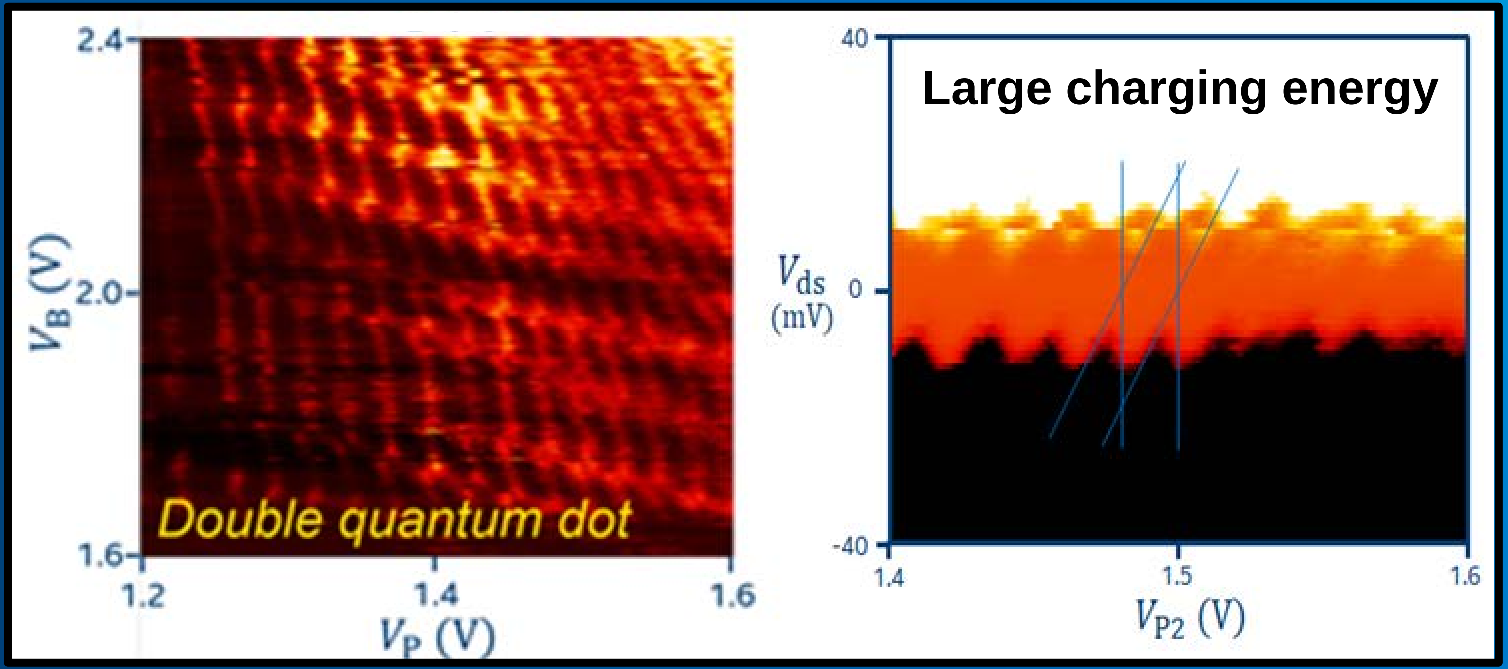
Ganging up multiple plunger and barrier gates can allow us to infer the gate dielectric interface quality

Quantum Dot Characterization at T=1.5K

Intel 300mm Substrate + Thermal Oxide + Academic Line process



Full 300mm Flow utilizing etched fins + scaled hi-k metal gate electrodes

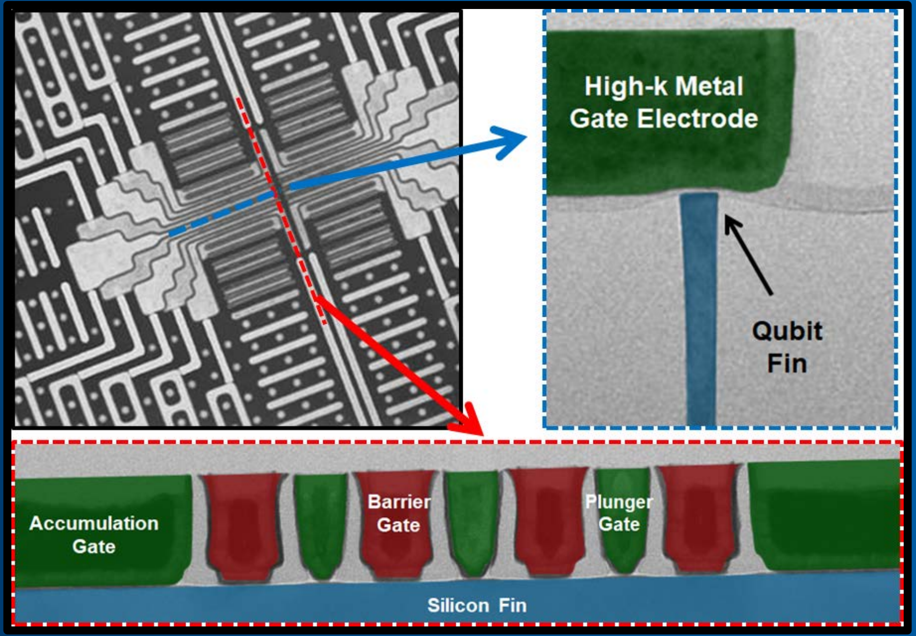


Intel substrate + thermal oxide give very clean data on the academic flow but show augmented noise on the full 300mm integrated flow

Unique Process Challenges for Qubits

Barrier Gate Interface:

- **Sees multiple etches (poly, spacer, etc…)**
- **Making a transistor in what is normally the S/D Contact**



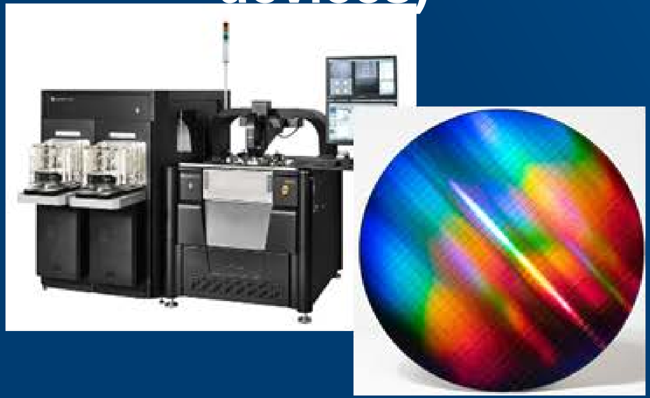
Thermal SiO2 Oxide

- **Done upfront post Fin etch**
- **Targeted on a narrow fin**
- **Gate oxide sees STI polish**

New innovations from etch/cleans, thin films and polish required to enable qubit manufacturing

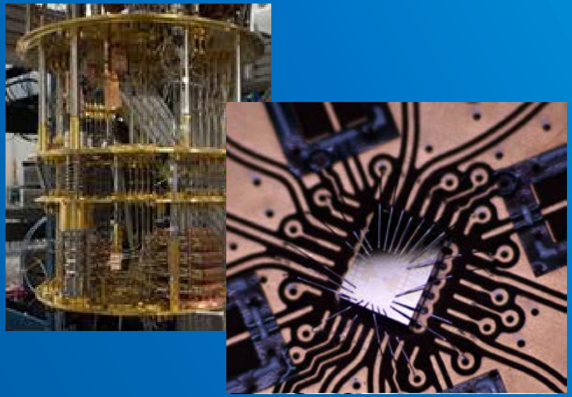
Quantum needs an Exponential Improvement in Low Temperature E-Test Throughput

Room temperature
1 hour/wafer
Huge volume (1000 devices)



T = 1.5 K
<u>12 hours/device</u>
+ several days for dicing & bonding

T = 10 mK
<u>Days/device</u>
+ several days for dicing & bonding

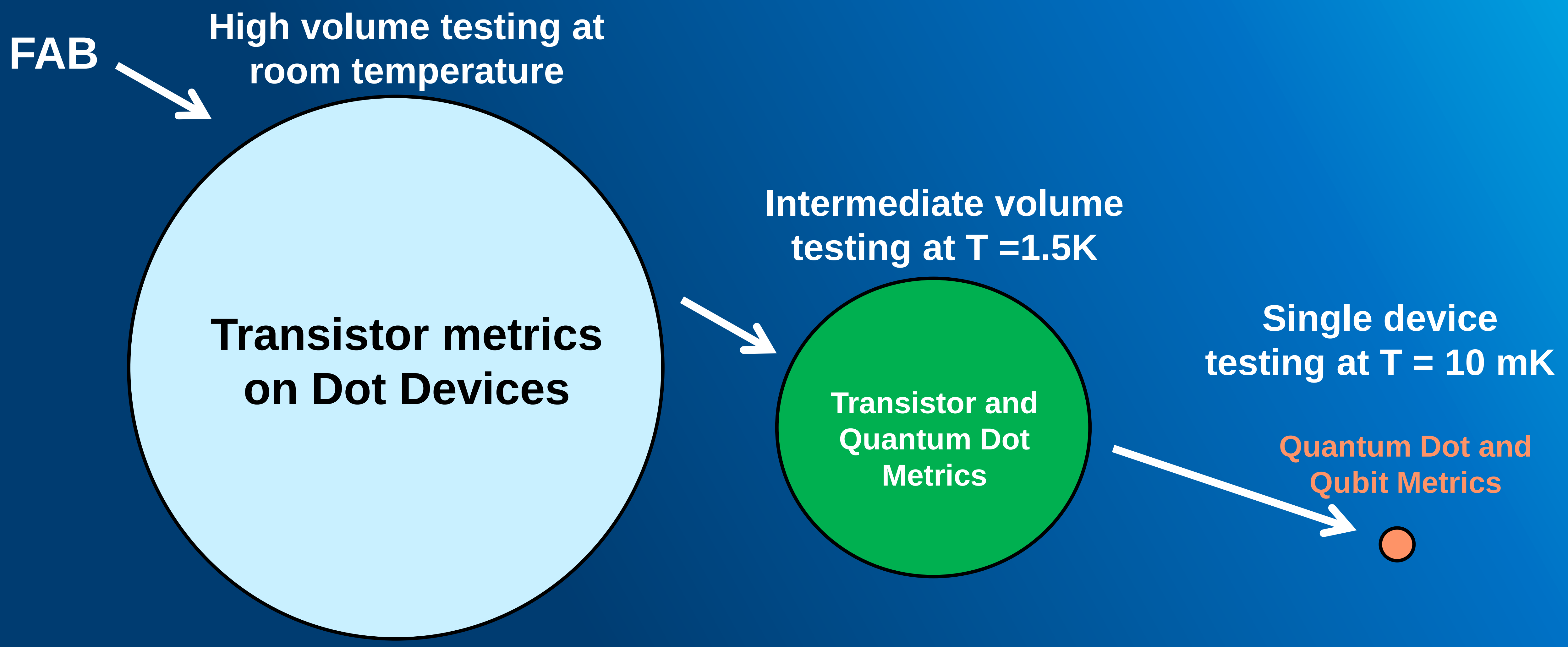


Increasing measurement time

Decreasing amount of data

Feedback cycle bottlenecked and too slow for Industry R+D

High Throughput e-test at 1.5K is Needed

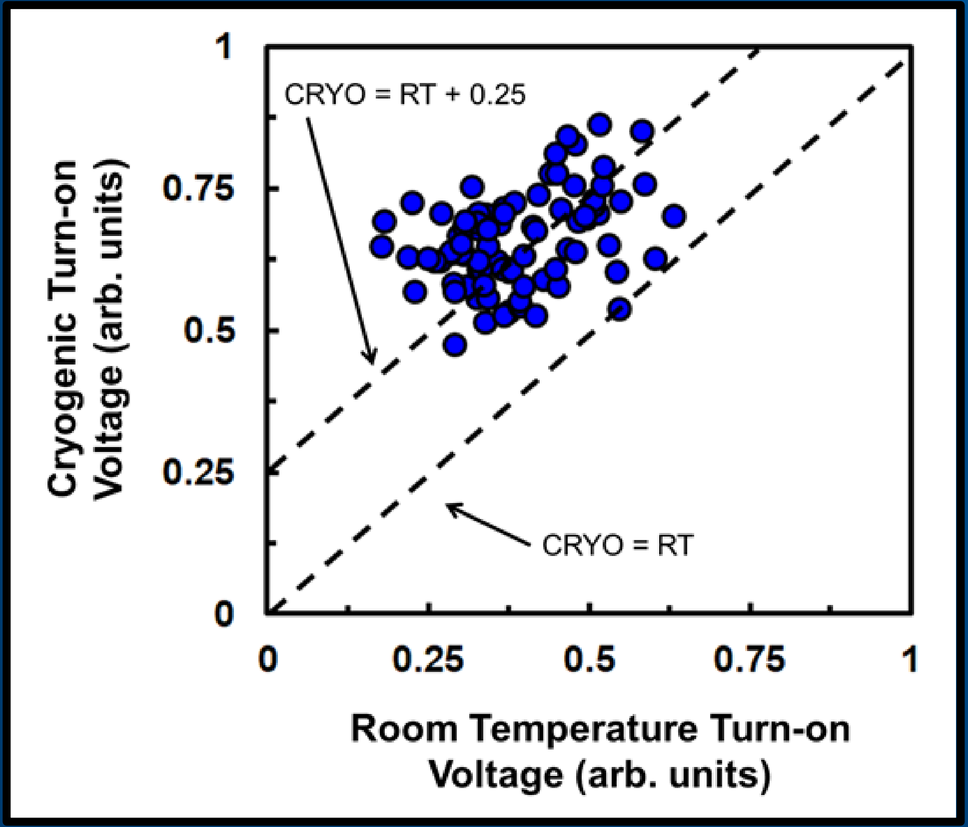


Enables screening and correlating data at RT, 1.5K and 10 mK

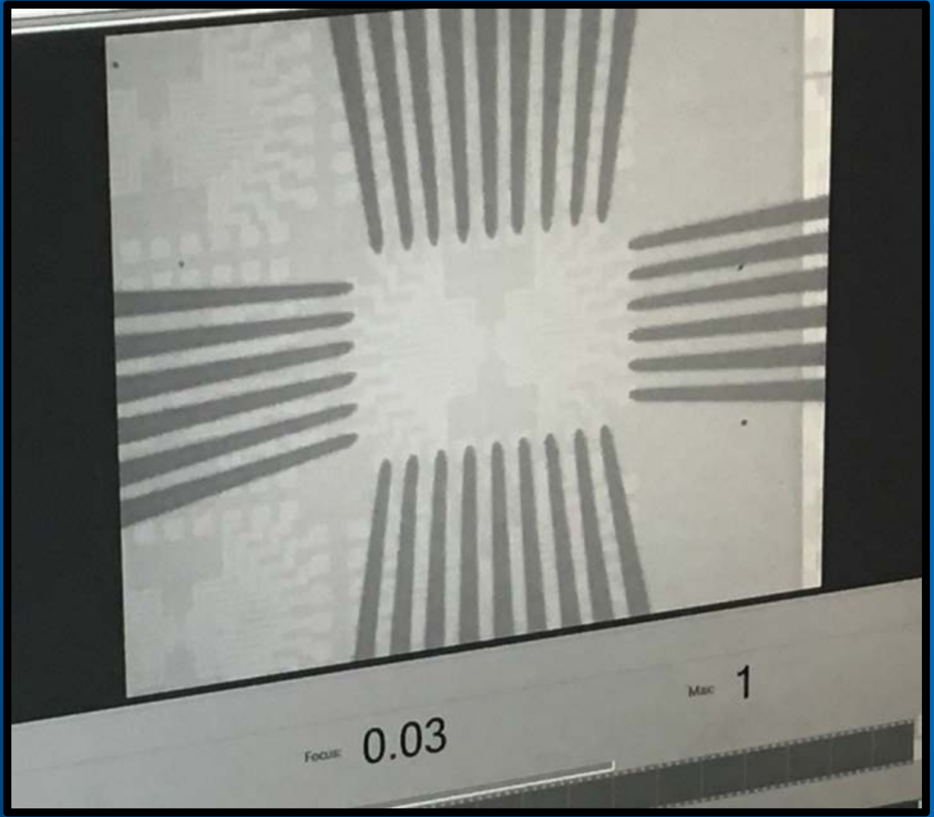
Driving Development of a First of Kind Tool for Cryogenic e-test Automation at T = 1.5K

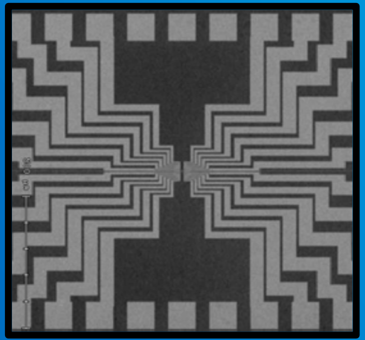
Intel Cryoprober Proof of Concept Data

Nested Gate VT



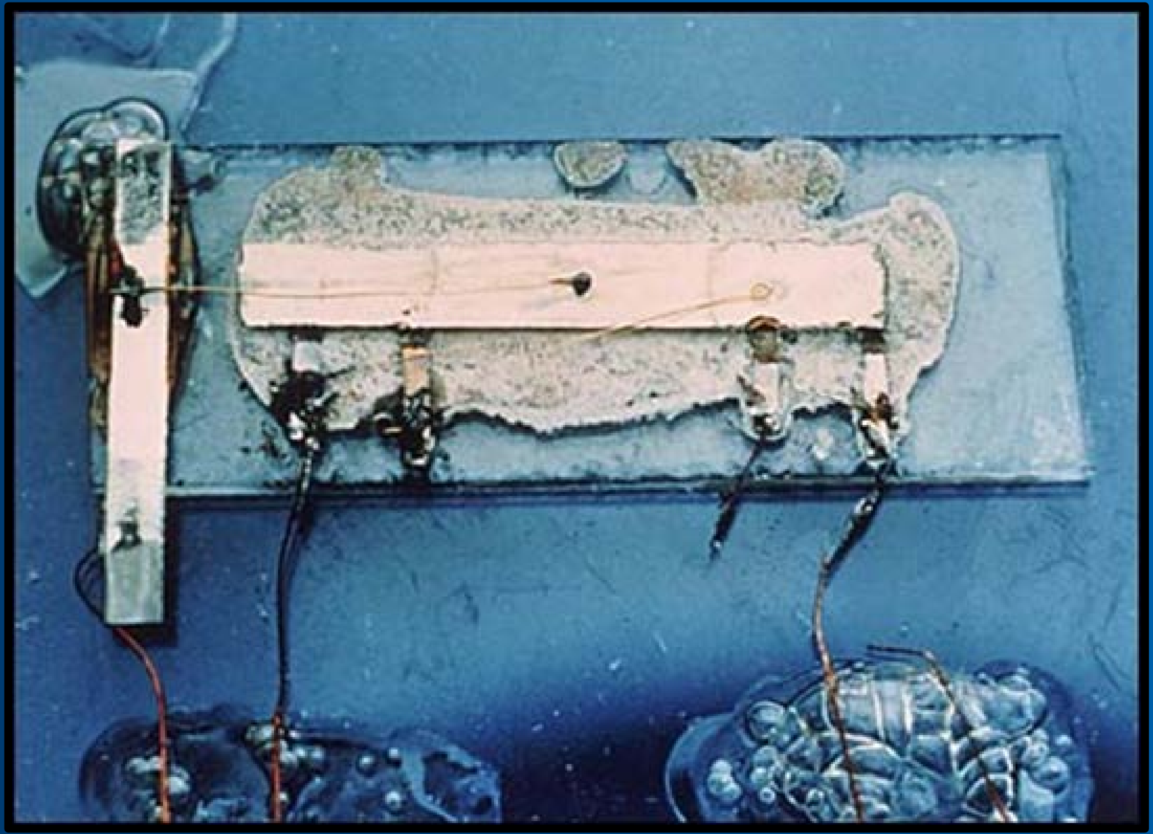
Prober camera on 7-gate testrow





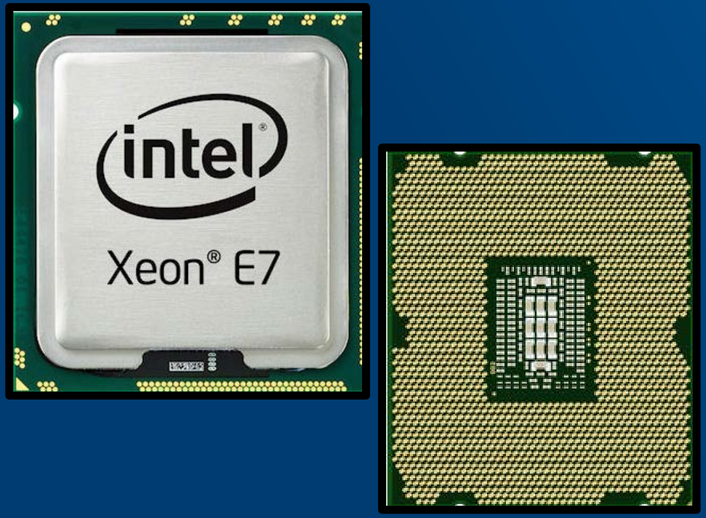
Statistical correlation of room temp to low temperature nested gate VT, with no variation increase at cryogenic temps

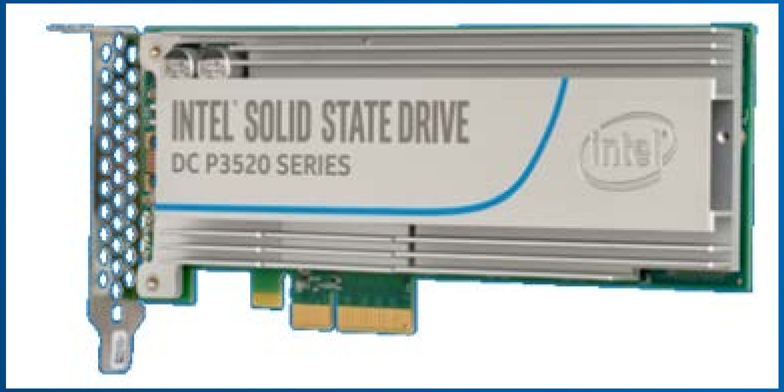
First Integrated Circuit (1958)

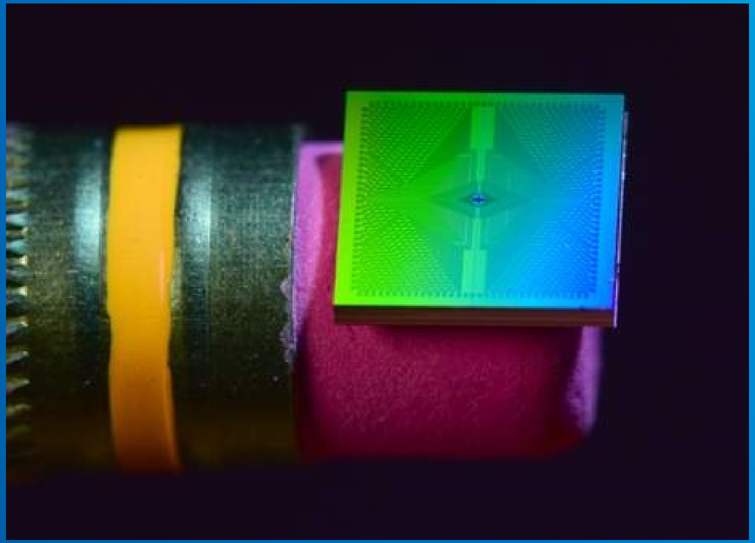


Brute force interconnection works for a few devices – but NOT millions

Rent's Rule and Scaling: $T=t*g^p$







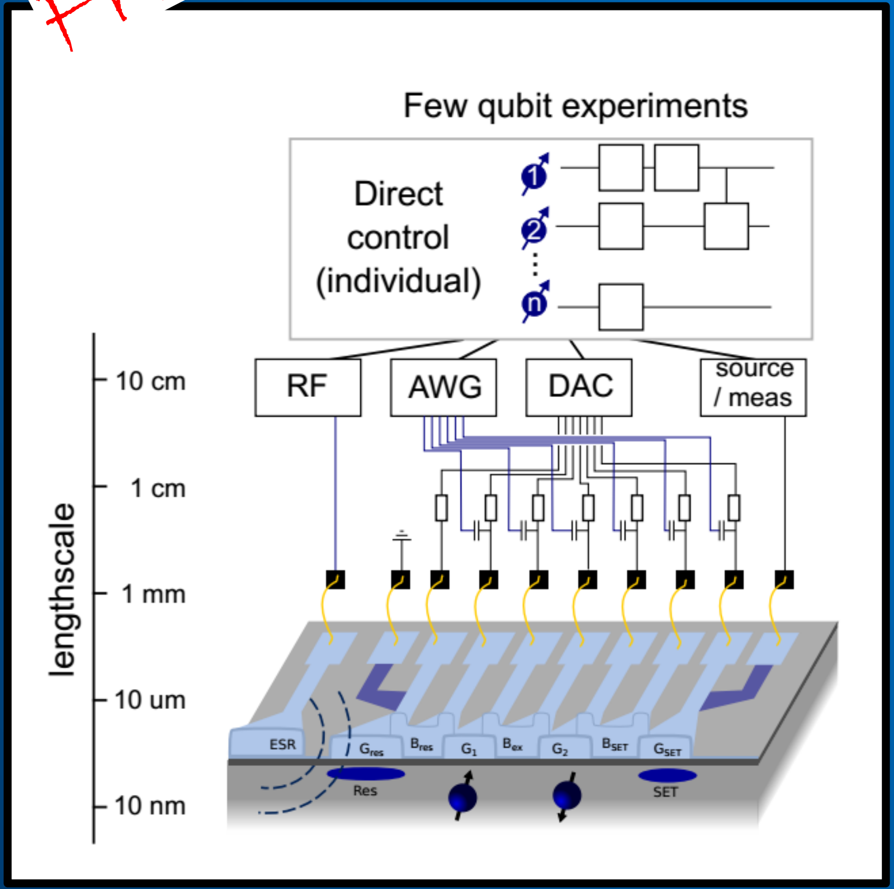
Processor
- 10^9 transistors
- 10^3 pins

3D NAND Memory
- 10^{12} bytes
- 10^2 pins

55 Gate Linear Dot Array
- Up to 26 Qubits
- 122 pins

Most overlooked discussion in the QC community!

Quantum Franke's Rule: $T=t*g^p$

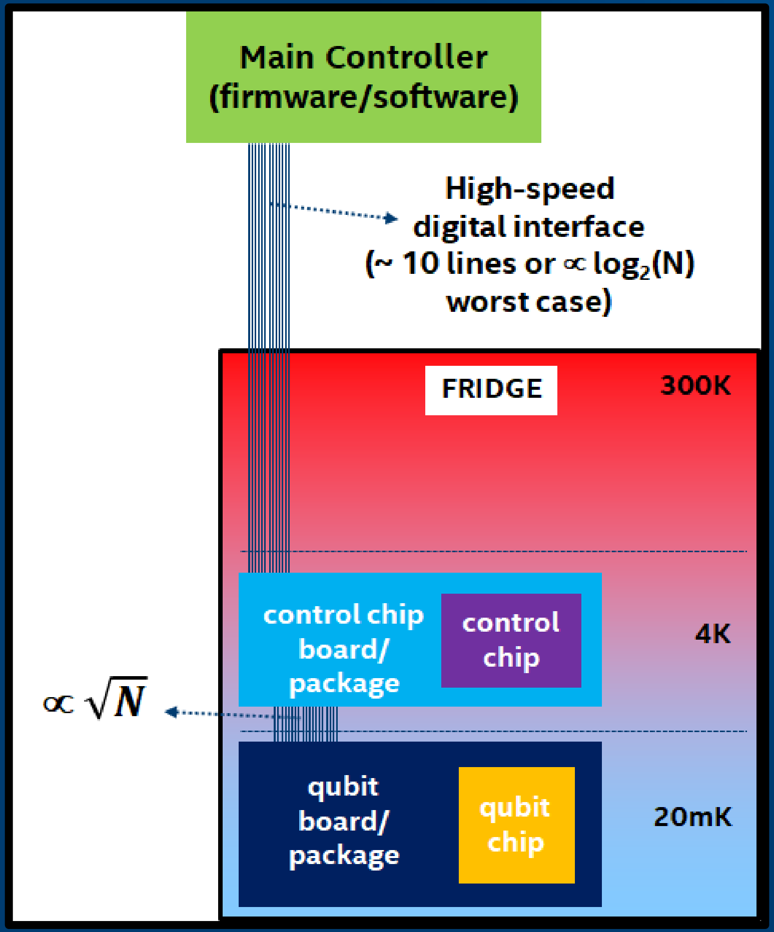


How to optimize "p" for quantum computing:

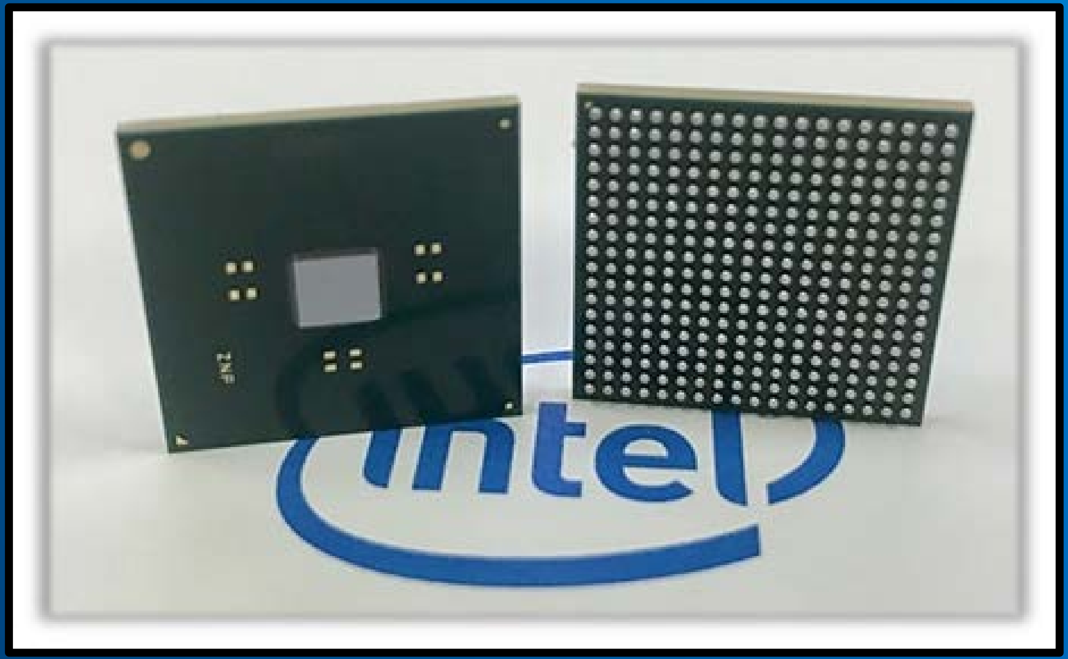
- Reduce wires out of the fridge (P_{fridge})
- Reduces number of I/O off of chip ($P_{I/O}$)
- Reduces number of wires per gate (P_{gate})

D. Franke et al. https://doi.org/10.1016/j.micpro.2019.02.006

Reduce Wires out of the Fridge: Cryo Control



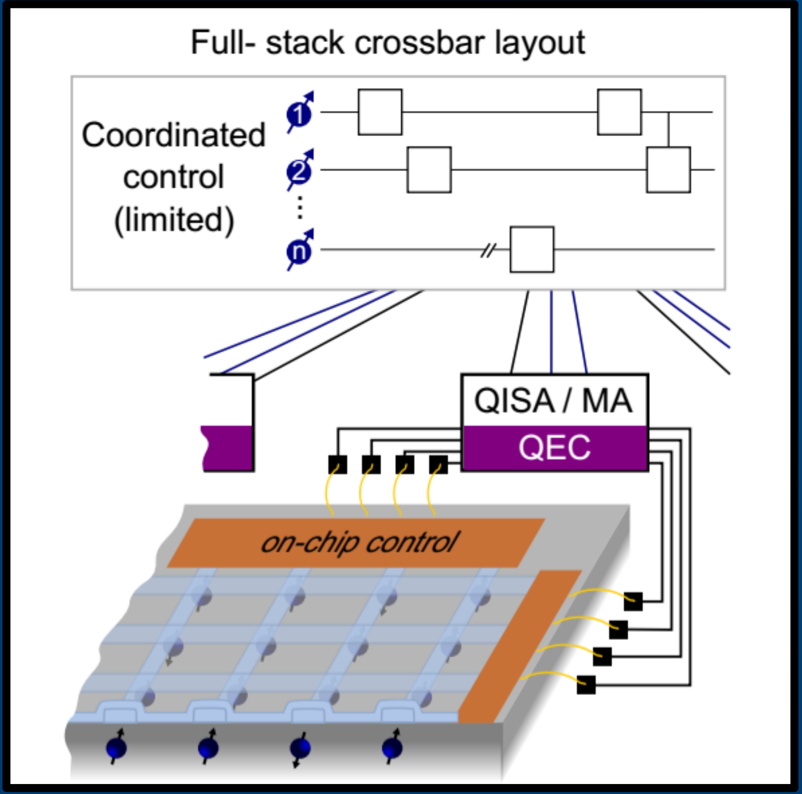
Custom Control Chip: Developed in Intel 22nm FFL FinFET technology with custom cryogenic analog/RF models



Frequency multiplexing to reduce connectivity and crosstalk mitigation to improve gate fidelity → In test at QuTech/DELFT

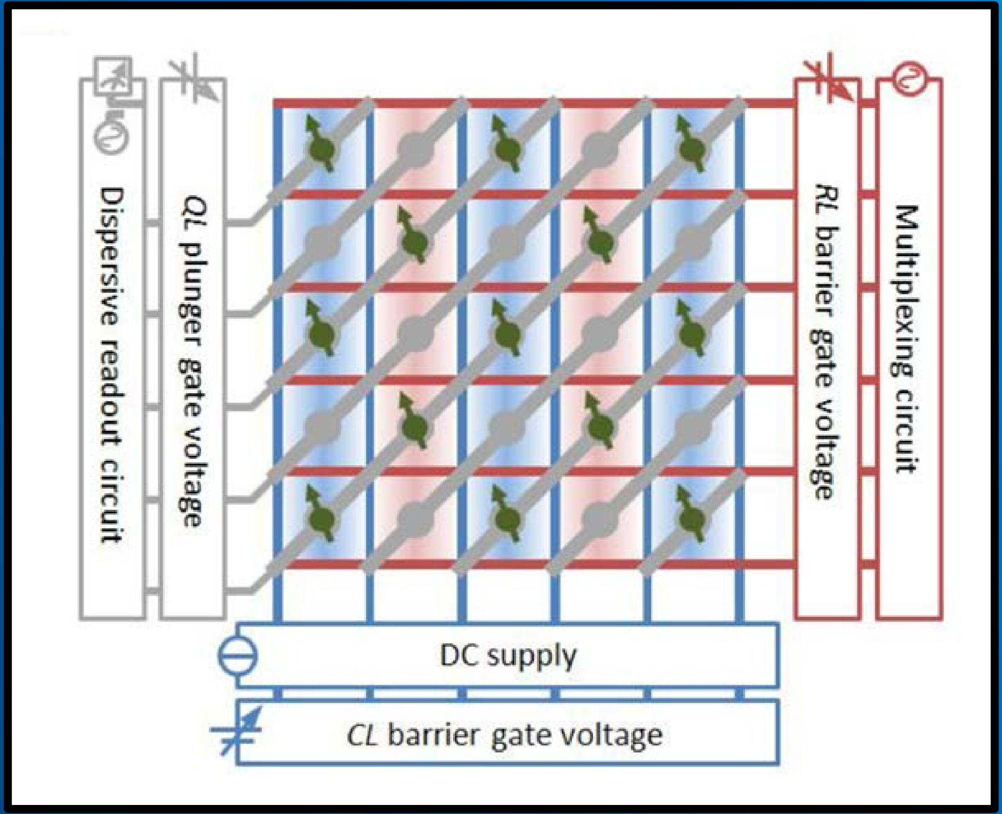
Reducing I/O per Chip and # of Gate Lines

On-Chip Multiplexing: reduces I/O per chip, but can heat sample requiring higher temp qubit operation



L. Petit et al. 10.1103/PhysRevLett.121.076801

Gate Selector Schemes: Orthogonal gates act as device selectors ; requires high uniformity



R. Li et al. 10.1126/sciadv.aar3960

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- **Interconnects and array scalability**

Intel is actively working on all of these!